FINAL TECHNICAL REPORT

L-BAND POWER MOSFET
CONTRACT #N00014-85-C-2064

1987

Submitted To:

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1.0 Introduction

L-Band power amplifiers for such applications as the TPS-59 phased array radar have used silicon bipolar transistors. The performance of power MOSFET's at VHF and UHF offered promise that there could be significant benefit for future L-band radars if their advantages could be extended to L-band. MOSFET's have demonstrated easier power combining and greater gain than their bipolar counterparts.

FET's offer several attractive features as microwave high power devices. Bias networks are uncomplicated and FET's can be employed in a simple pulsed generator mode saving costly circuit switching elements. In contrast to the bipolar device, the drain current of the FET has a negative temperature coefficient at high current levels, therefore it has the tendency to be thermally stable and can typically withstand higher VSWR mismatches. Since the FET is a majority carrier device it exhibits lower noise floor characteristics. FET's are basically square law devices and can be expected to be more linear with smaller intermodulation and cross modulation products.

FET amplifiers provide the linearity of class AB operation with simpler bias circuits. The high DC gate impedance, relatively linear operation, and gate control capability make the silicon power FET a desirable device.

Previously available power MOSFET's have been

constructed using aluminum metallization. However, since gold has been a standard in the microwave industry because of enhanced reliability, a need for gold metallized L-band power FET's was identified.

The goal of this development program was to produce a medium power (10W) L-Band MOSFET whose die is similar in performance to the TPS-59 output device. The PH8592 provides 55W at 7.4 dB gain and minimum efficiency of 52%. Typical efficiency is 55-60%. The driver device shows 7.8 dB gain and 46% efficiency. Generally, a tradeoff between gain and efficiency is possible.

The goals of the contract have been met. A MOSFET cell having capability similar to that of the TPS-59 transistor cells has been developed. A gold metallization process has been developed and applied to the cell. A 10W transistor demonstrating TPS-59 levels of performance has been developed. Figure 1.0-1 summarizes the contract goals, and performance of the MOSFET developed.

1.1 Approach

An L-Band DMOS FET geometry was employed during this development. The design of this device is described in section 2.1. Numerous process innovations were implemented and evaluated. During the course of die development, the channel length was greatly reduced, the metallization was changed, and thick oxide plugs and a split-polysilicon geometry were introduced. Power was increased from 1.1 watts per cell to 4 watts per cell and F_T increased from 1.4 to 4

PERFORMANCE SPECIFICATION GOALS

TASK III - 10W TRANSISTOR

PULSED POWER	>10 WATTS
PULSE WIDTH	2 mS
DUTY CYCLE	20%
GAIN	7-10 dB*
EFFICIENCY	>55%*
FREQUENCY	1215-1400 MHz
VSWR	>3:1
RETURN LOSS	>10 dB

*Contract goal is performance comparable to TPS-59 transistors. The gain and efficiency numbers are typical of TPS-59 drivers at 10-25W.

Figure 1.0-1 Contract goals. The optimized ML1 MOSFET transistors meet the contract goals.

GHz. These die were extensively characterized and the results are described in section 2.2.

Both aluminum and gold metallized FET's were fabricated and both types were included in the deliveries. The use of a polysilicon gate and a refractory metal barrier layer prevents contamination of the channel by gold ions so that the potential for increased reliability due to gold metallization can be realized.

1.2 Performance

The contract goal of a 10W MOSFET transistor with performance comparable to that of TPS-59 bipolar transistors was met. Power of the optimized cells was somewhat higher than the minimum so the final devices delivered were characterized at 12.5W. Figure 1.2-1 shows broadband performance of a typical device operating under the TPS-59 duty cycle of 2 ms and 20%. At the lower power of 10W, gain is somewhat higher and efficiency is somewhat lower.

All measurements were made with continuous gate bias. Use of pulsed bias would permit improved efficiency.

1.3 Packaging and Construction

A new package was designed to permit distributed matching of the transistors and a unique input matching structure that we believed necessary to match the FET. The package performed well electrically, and was used during development, but the final devices used more conventional packages.

The MOSFET input was capacitive, so a shunt-L input

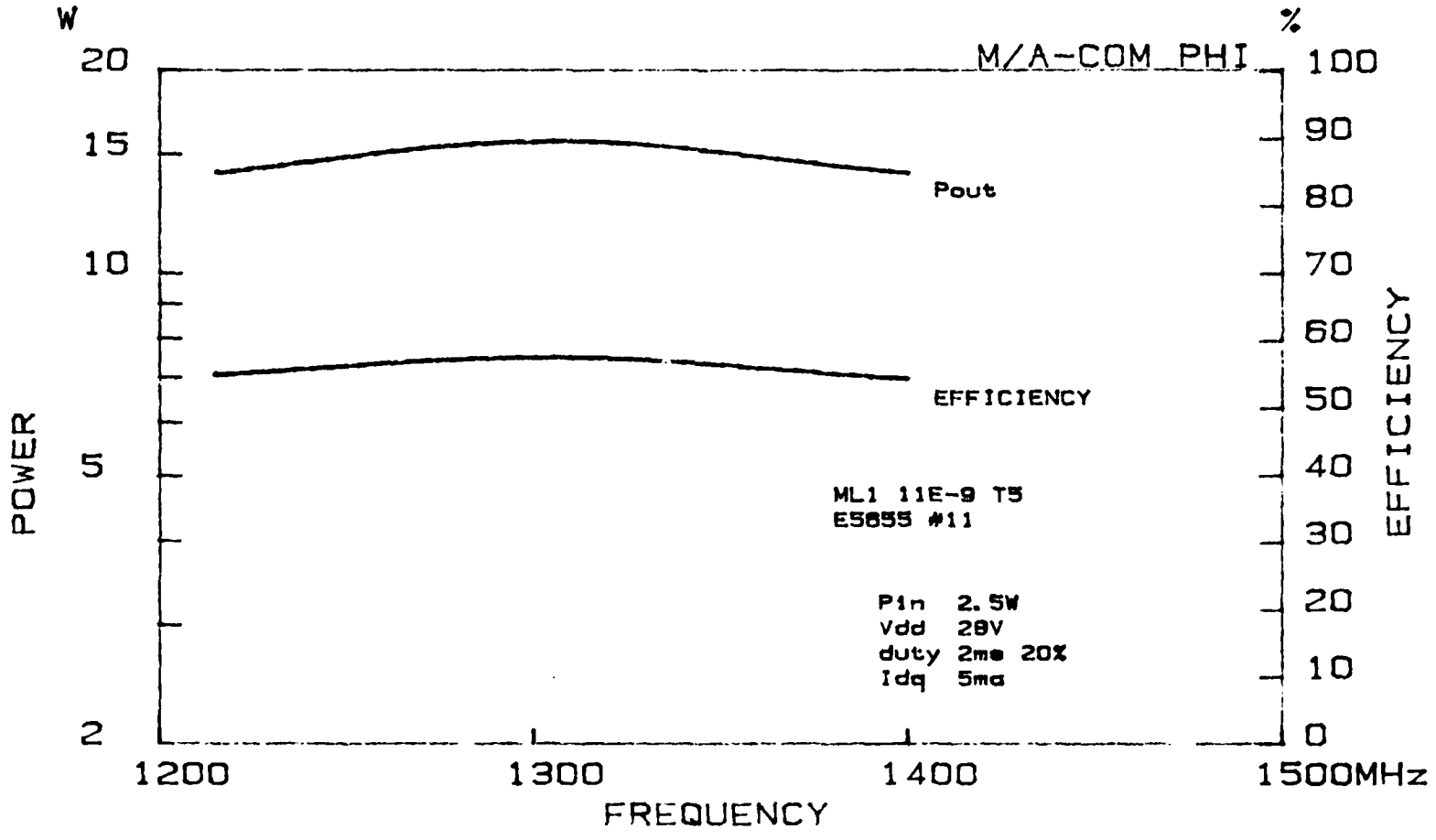
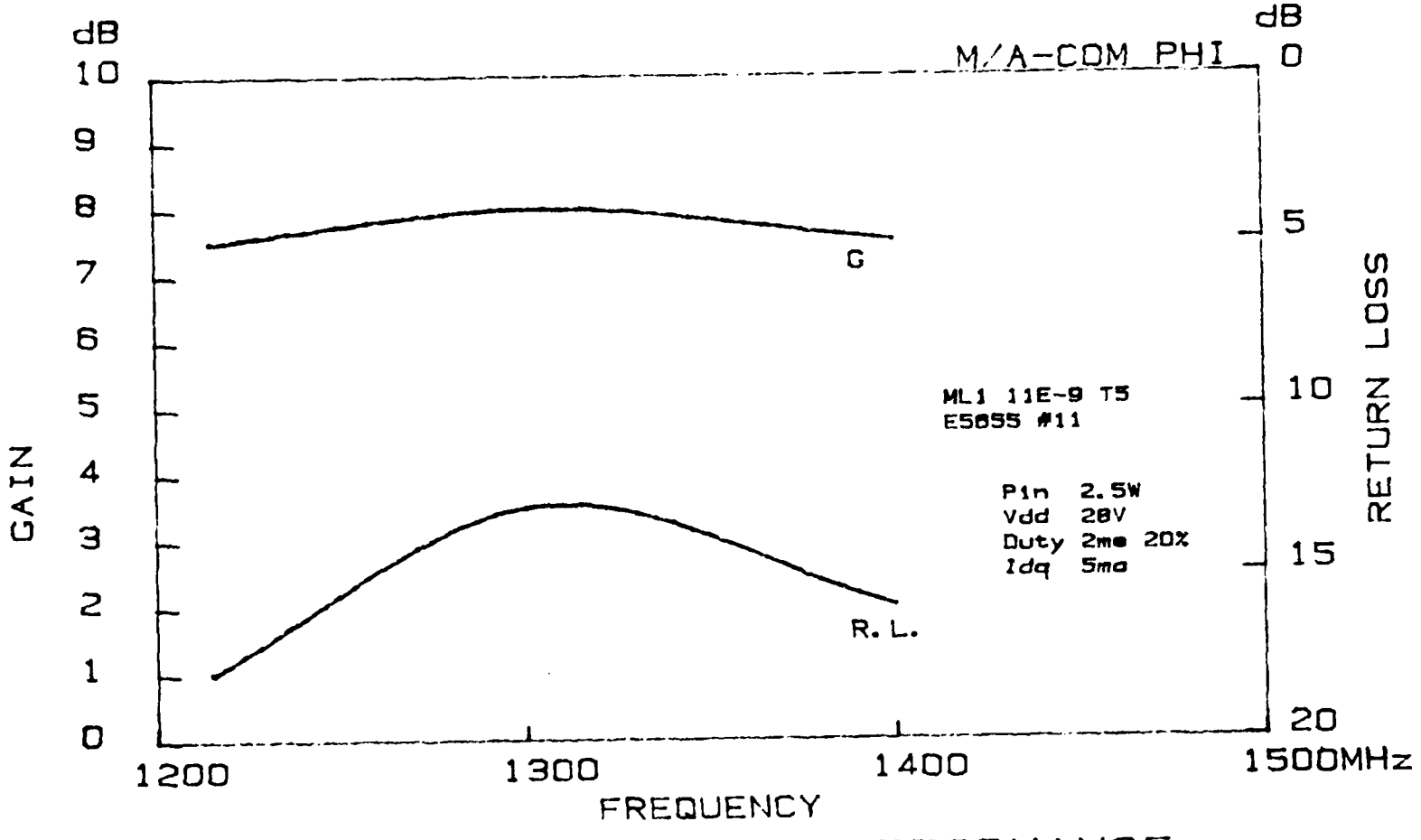


FIGURE 1-2-1a. OUTPUT POWER AND DRAIN EFFICIENCY OF MOS TRANSISTOR DEVELOPED DURING THIS CONTRACT



BROADBAND MOSFET PERFORMANCE

FIGURE 1.2-1b. GAIN AND RETURN LOSS OF L-BAND MOSFET. THE CONTRACT GOALS WERE MET

match was used instead of the low pass match commonly used in bipolar devices. However, it was not necessary to use an unorthodox package.

1.4 Delivered Items

The Statement of Work provides that 10 L-band devices are to be delivered at the conclusion of each of the three tasks. Appropriate fixtures for evaluating the devices at NRL are also required.

The requirements have been met, as summarized in Table 1.4-1. The Task I and Task II devices are single cell parts with no interval matching. Test Fixture 862-441 is for evaluating them at the most critical frequency, 1.4 GHz.

Task II devices are internally matched 4 cell parts. Test Fixture 872-448 is for evaluating these parts over the specified 1.215 to 1.4 GHz band. These parts meet the power and gain requirements across the band. Not all of the parts meet the 55% efficiency goal over the entire band. For some parts, efficiency drops to 53% over part of the band. The performance of the delivered items is discussed in Section 2.2-5.

In addition to the 30 specified devices, 10 additional Task II devices and 5 additional Task III devices were delivered. These can be evaluated in the same test fixtures, and were delivered to demonstrate some of the processes, such as gold metallization, developed during this effort but not incorporated in the optimized device.

TABLE 1.4-1

DELIVERED ITEMS

	Lot	Quantity
Task I 1 cell	E 5935	10
Task II optimized 1 cell	E 5962 E 5963	10 10*
Task III low broadband	E 5655) E 5960) E 5964	10 5*

*These additional devices were delivered to demonstrate alternatives evaluated during the development effort.

2.0 Die Development

2.1 ML1 DMOS FET

2.1.1 Introduction

Two factors contributed to the ML1 DMOS FET as the initial die choice for this study. First, the goal of the contract was to copy the cell layout of the bipolar device employed in a production of the TPS-59 radar. Thus, the advantage of a continual comparison between bipolar and FET technology would be obtained. Second, the configuration and cell design employed provided an excellent vehicle for evaluating variations and innovations in both wafer processing, and the details of the mask design.

M/A-COM PHI has committed to the polysilicon gate Double diffused Metal Oxide Silicon (DMOS) FET as the base technology for its microwave power MOSFET product. The highly doped phosphorous polysilicon gate acts as a credible conductor for gate current and also acts as a getter for mobile ions. Thus, it facilitates implementation of gold metallization which is used extensively during this work.

Sections 2.1.2 and 2.1.3 describe the basic internal cell structure and cell layouts respectively. The remainder of the section addresses design improvements such as advanced epitaxial techniques, double level metal for capacitance reduction, C_{rss} reduction techniques and channel length issues.

2.1.2 ML1 Cell Cross Section

Figure 2.1-1 illustrates the device cross section. Metal fingers and polysilicon stripes are defined in an interdigitated fashion, thus Figure 2.1-1 simply represents a vertical slice through the die perpendicular to the fingers. Source metallization forms a body short between the P type boron implant and diffusion and the shallow N+ arsenic source implant and diffusion. The drain contact is formed via the bottom of the chip which connects to the N- exitaxial material. 100 direction epitaxial material is employed such that surface channel mobility is maximized. Since the gate polysilicon is highly phosphorous doped and therefore conductive, the channel is formed by inverting the P region at the surface of the silicon under the gate oxide between the N+ source diffusion and the epi drain. Figure 2.1-2 shows an expanded view of the channel region and the resultant current flow which would occur under proper positive bias. Since this device is fully implanted, the process flow for the polysilicon etch and edge definition determines implant placement for both the boron P type body implant and the arsenic N+ source implant. Thus, the channel length is defined along the surface as the P-diffusion between the drain and N+ source diffusion.

Pitch distance and polysilicon gate width discussed in the next section are shown in Figure 2.1-3. Optimizing these dimensions with respect to epitaxial resistivity and photolithography limitations was a major task for this

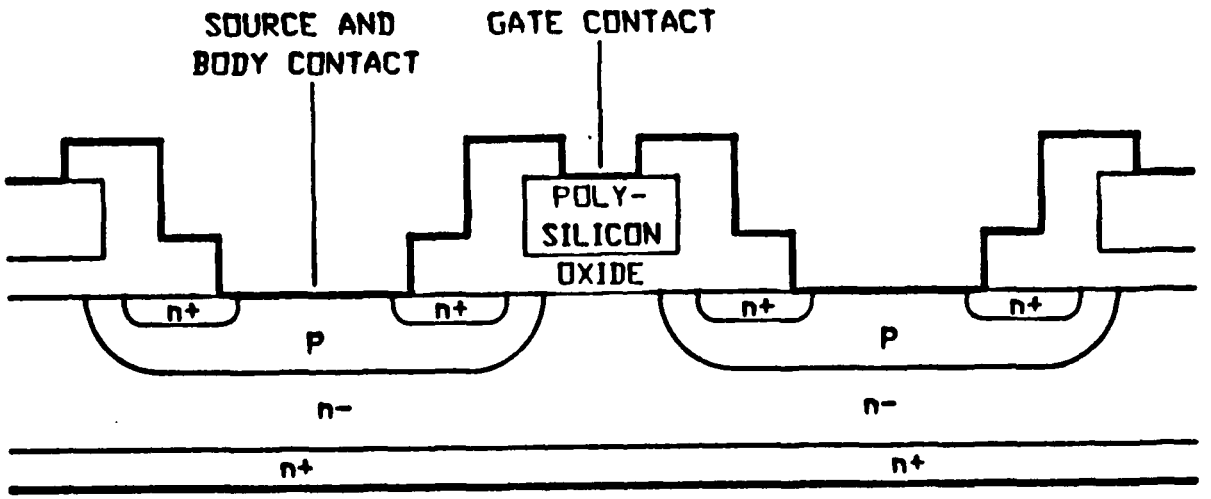


FIGURE 2.1-1 VERTICAL CROSS SECTION

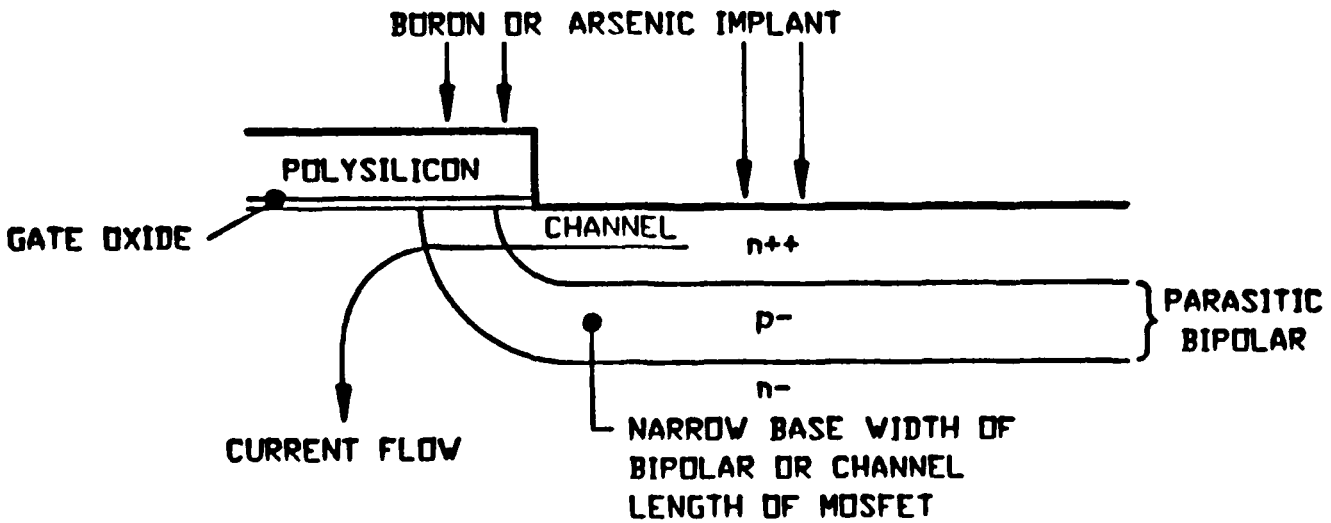


FIGURE 2.1-2 EXPANDED VIEW OF CHANNEL

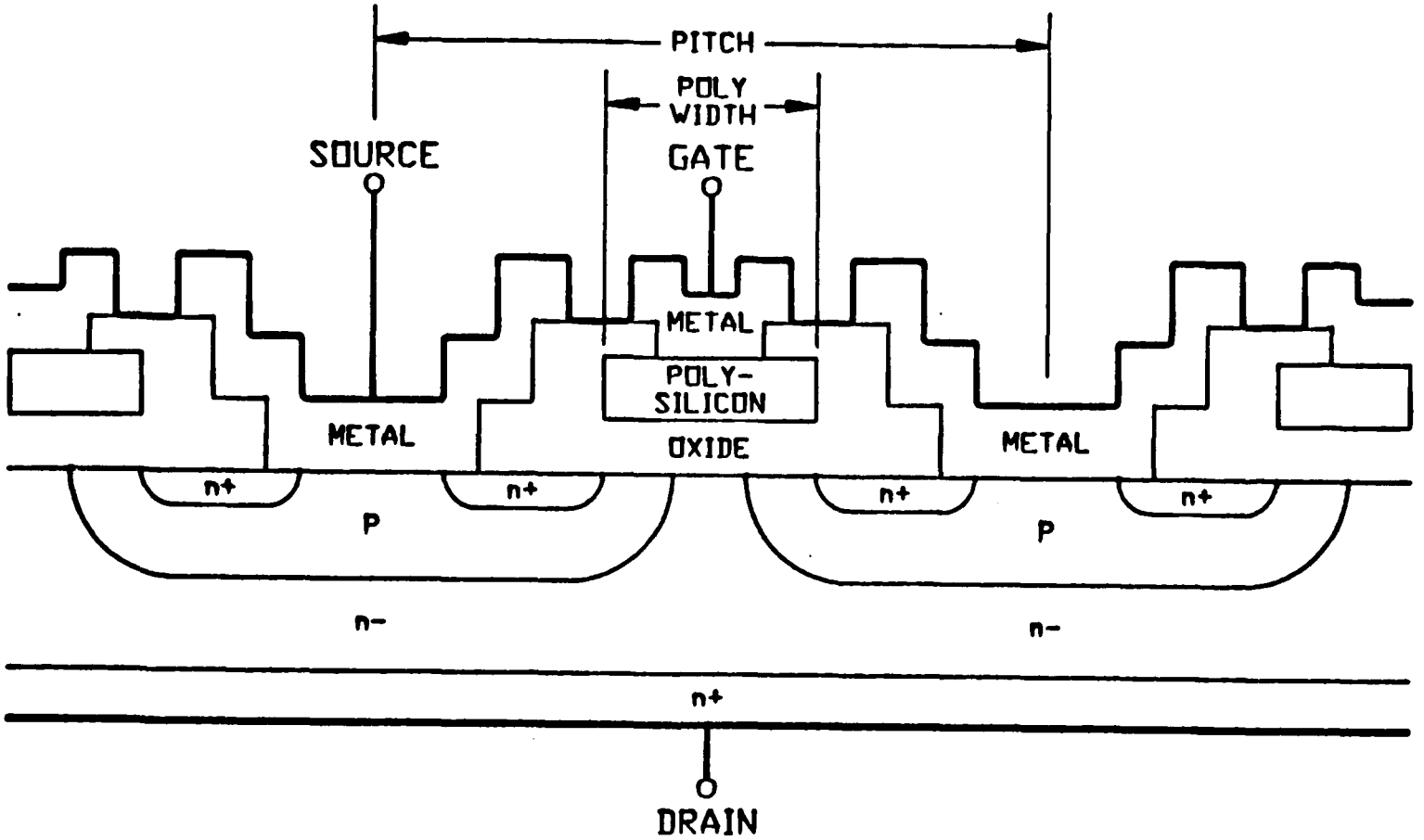


FIGURE 2.1-3 DEFINITIONS PITCH/POLYWIDTH

contract because of the unknown effect of the JFET that is formed in the epi below the gate oxide as shown in Figure 2.1-4. This series JFET occurs since the depletion resulting from the bias of the P- region tends to pinch-off the current flowing from the channel into the drain region. Section 2.2.4 addresses this problem in detail. Since the range of the depletion region is directly influenced by the epitaxial resistivity, polysilicon width vs epitaxial resistivity becomes a performance optimization issue. Combining the dimensions of the polysilicon width and the pitch, which defines the distance between source and gate fingers, gives a design figure of merit which describes the total amount of gate width per active source area. Gate width within an active cell defines the total linear periphery of current carrying elements within an active source area. Thus, gate width to source area (equivalent to the bipolar figure of merit of emitter periphery to base area) is a packing density figure of merit which should be maximized in order to reduce output capacitance for a given amount of output power. However, for the DMOS design employed, the JFET effect limits gain, power and efficiency performance for tight geometries as discussed in section 2.2.2. Thus, the JFET effect was eventually found to be one of the fundamental limitations of this design.

2.1.3 Cell Layout

Figure 2.1-5 illustrates four cell layout designs employed in the mask set. Cell types 1, 2 and 3 are

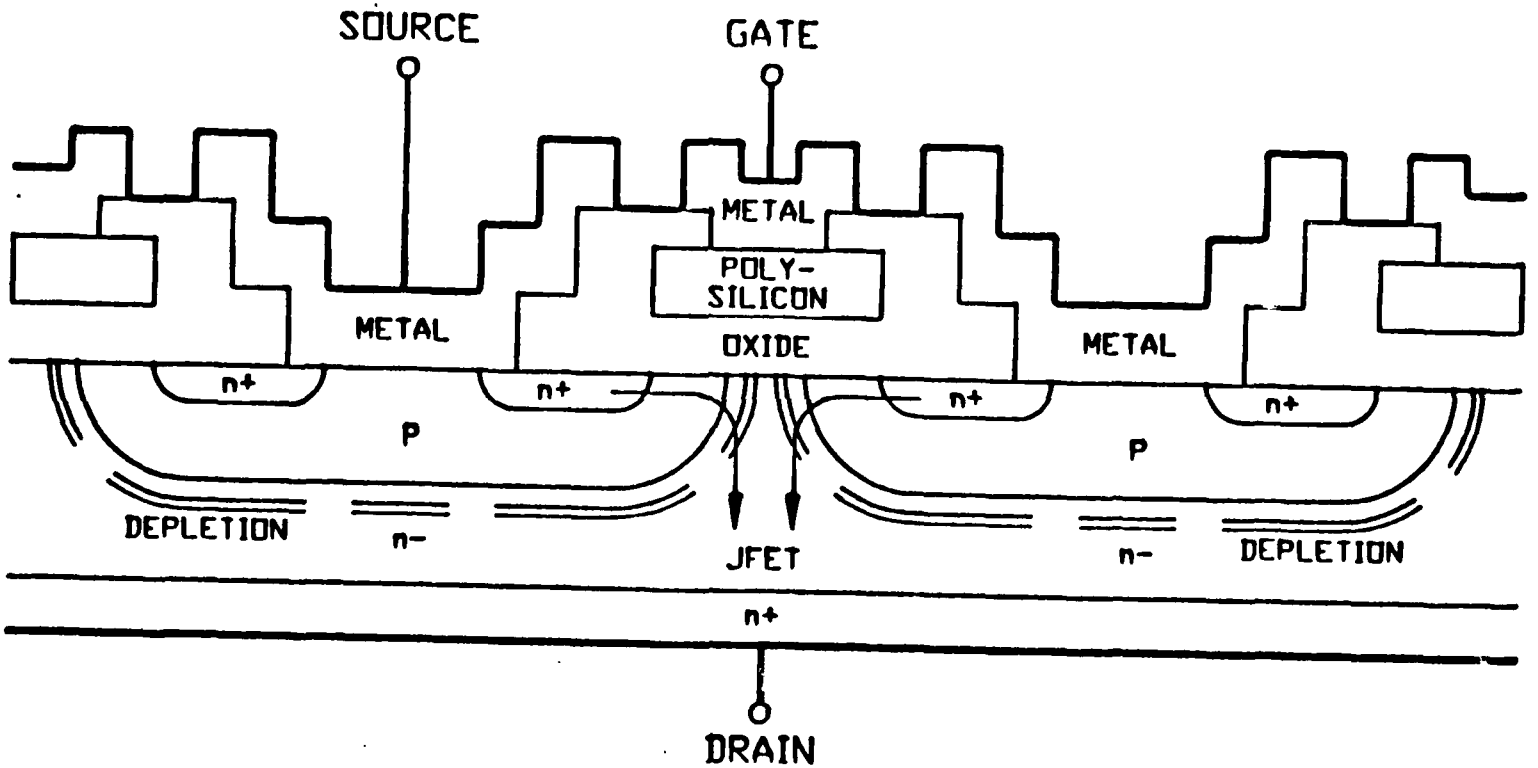


FIGURE 2.1-4 PARASITIC JFET FROM P-DEPLETION

GATE WIDTH	.40 CM	.20 CM	.25 CM	.33 CM
PITCH	.65 MILS	.90 MILS	.65 MILS	.50 MILS
POLY WIDTH	10.0 MICRONS	12.5 MICRONS	10 MICRONS	8 MICRONS
SOURCE AREA	56 MILS^2	40 MILS^2	40 MILS^2	40 MILS^2

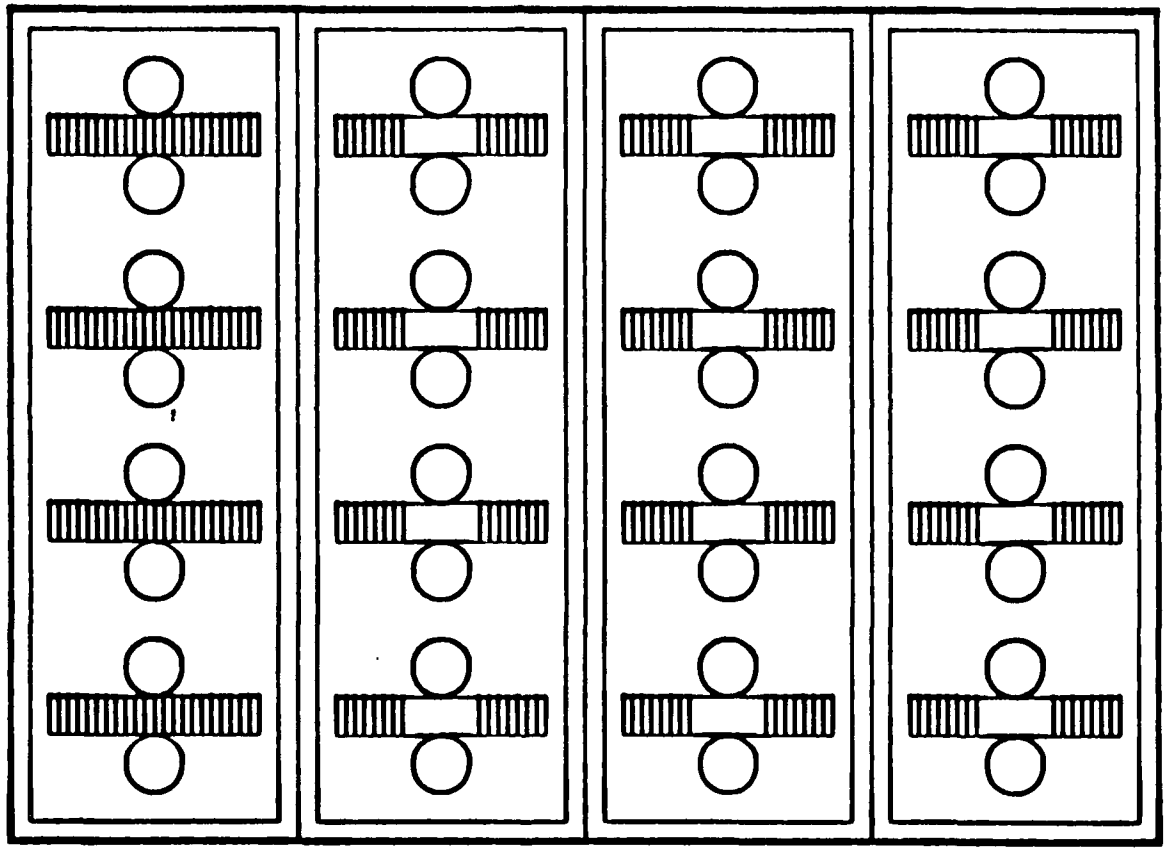


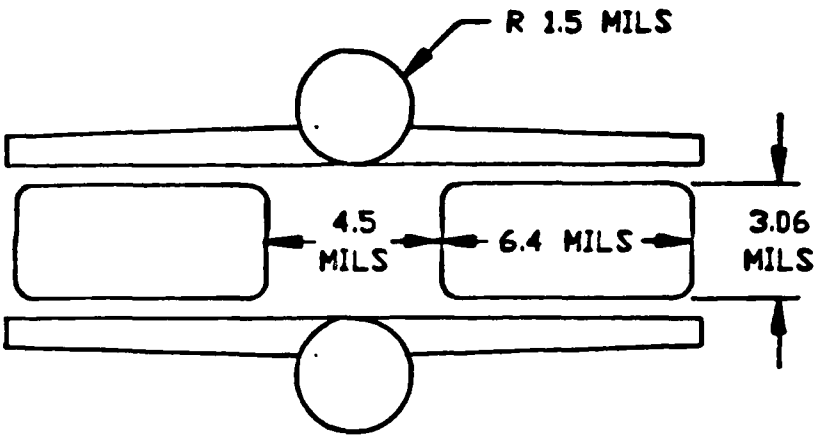
FIGURE 2.1-5 FOUR DIE TYPES ON THE ML-1 MASK SET

identical in source area (40 mil^2) but each has a different pitch and polysilicon width. Type 5 has the same polysilicon width and pitch but fills in the area between the active areas in order to increase the total active source area by 40%. Figure 2.1-6 illustrates the active area and pad metallization dimensions.

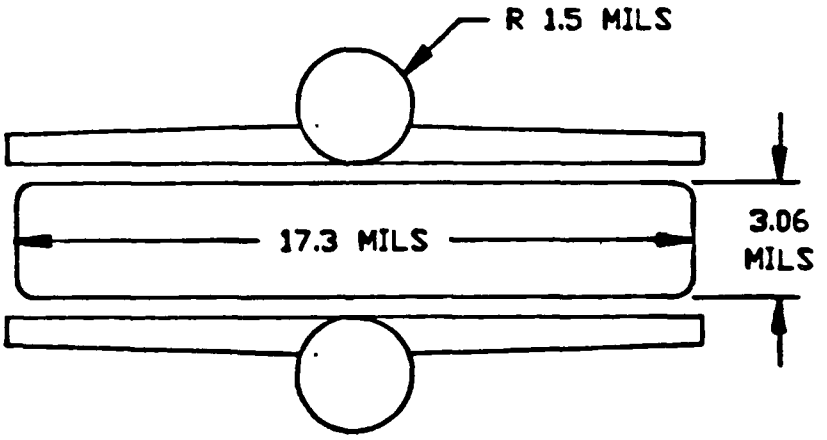
Each group of 4 cells connected by gate and source pads is defined as a chip for the purposes of future discussions. Cells are considered two active source areas connected by bonding pads except for the type 5 case which has one active area. Scribe lines separate each chip and the pattern represented in Figure 2.1-5 is repeated across the entire wafer. Thus, each epitaxial wafer in the lots processed for this contract was able to yield a true study of epitaxial resistivity vs geometry since processing for each wafer was reasonably identical.

2.1.4 Device Structure and Processing

Processes and device geometries for a self-aligned short channel vertical DMOS FET are described in this section. Since depletion mode channels can easily be made with adjustments to the doping profiles, only enhancement mode devices will be discussed below.



TYPES 1, 2, AND 3



TYPE 5

FIGURE 2.1-6 DMOS CELLS AND PAD DIMENSIONS

STEP

1) Starting material - vertical DMOS

-1 ohm-cm

-100 direction

Mesa formation

-Grow 500 A oxide

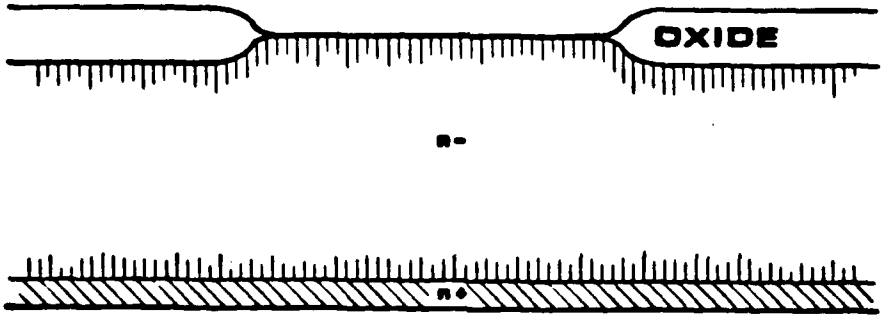
-Deposit 1000A nitride

-1st mask - oversized active area covered with PR

-Etch nitride from field

-Grow one micron of field oxide

-Remove nitride and thin oxide



2) Define gate area

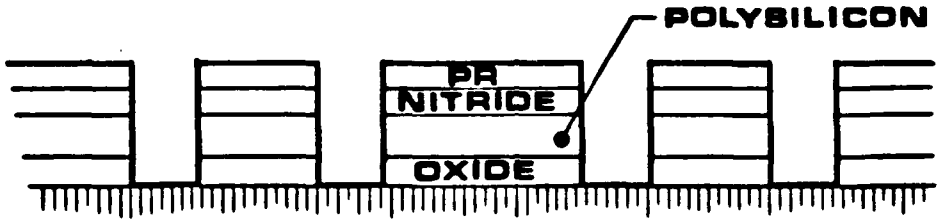
-Grow gate oxide

-Poly deposit and dope

-Deposit nitride

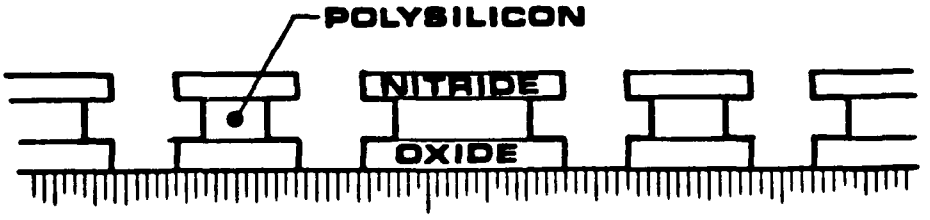
-2nd mask - dry etch

-Boron implant



3) Define overhang

-Wet etch or isotropic dry etch the poly



4) Fill in boron implant

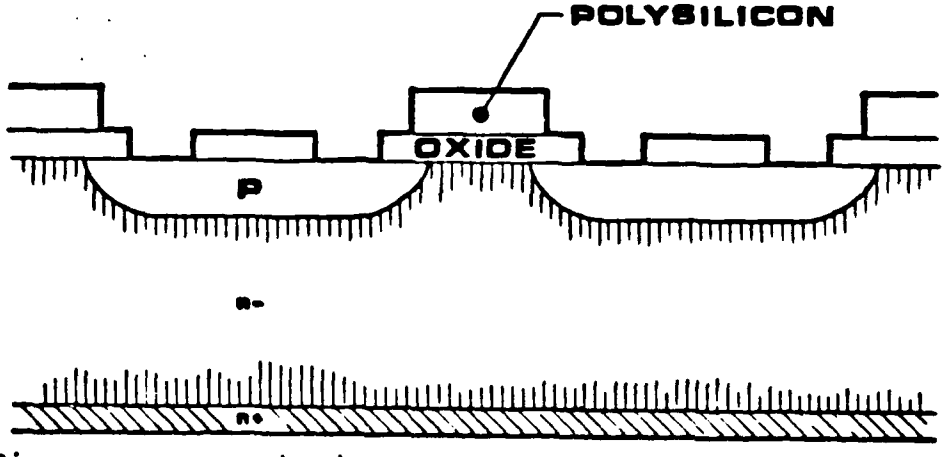
-3rd mask - oversized body

-Etch nitride

-Etch poly - leave gate oxide

-Boron implant

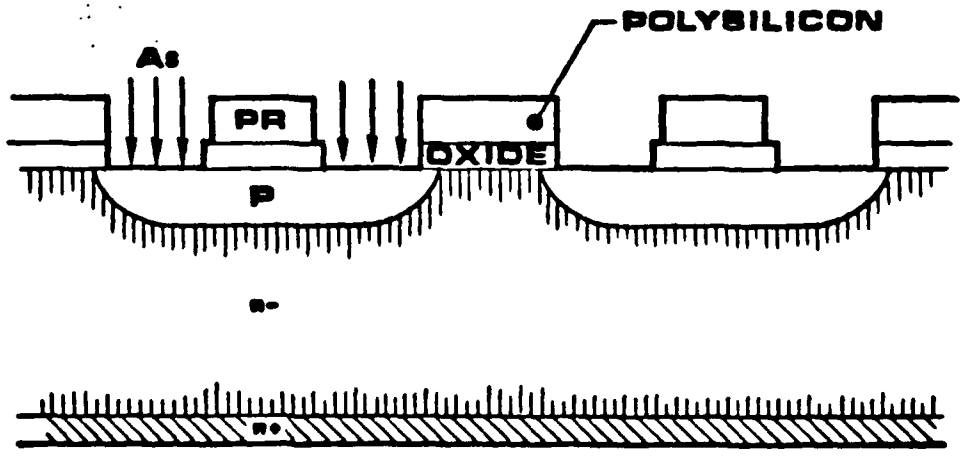
-Boron diffusion 1.5-2 microns



5) Define source contact

-4th mask - cover body contact and field

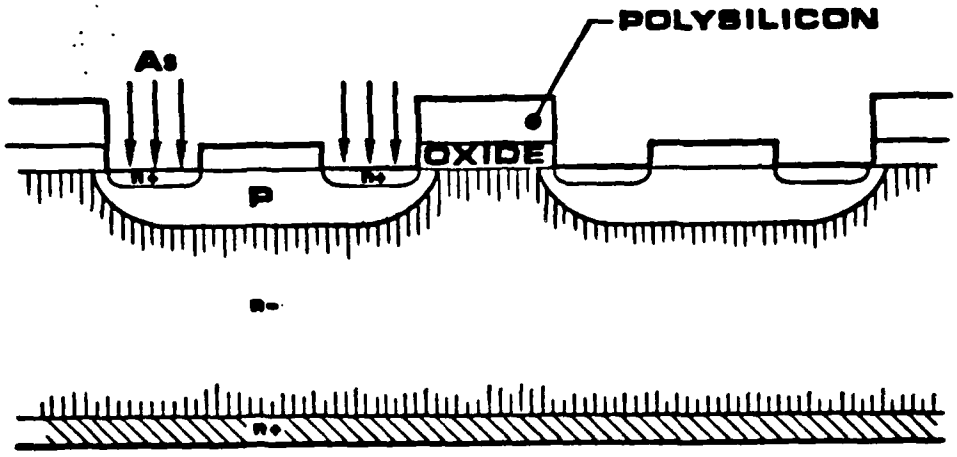
-Arsenic implant



6) Gate formation

-Arsenic anneal

-Diffusion

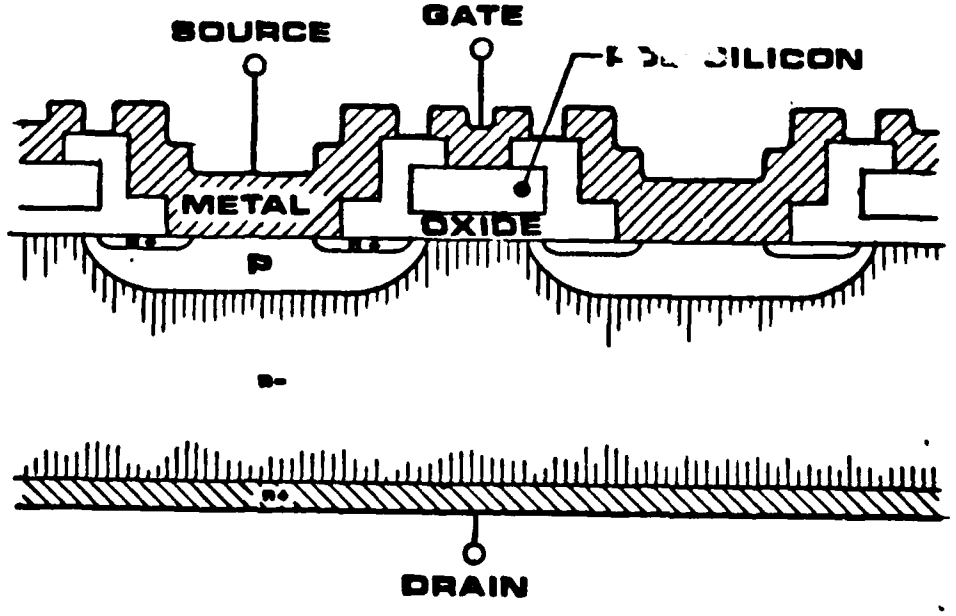


7) Sandwich of deposited oxide and nitride

Contact formation

-Mask 5

-Dry etch

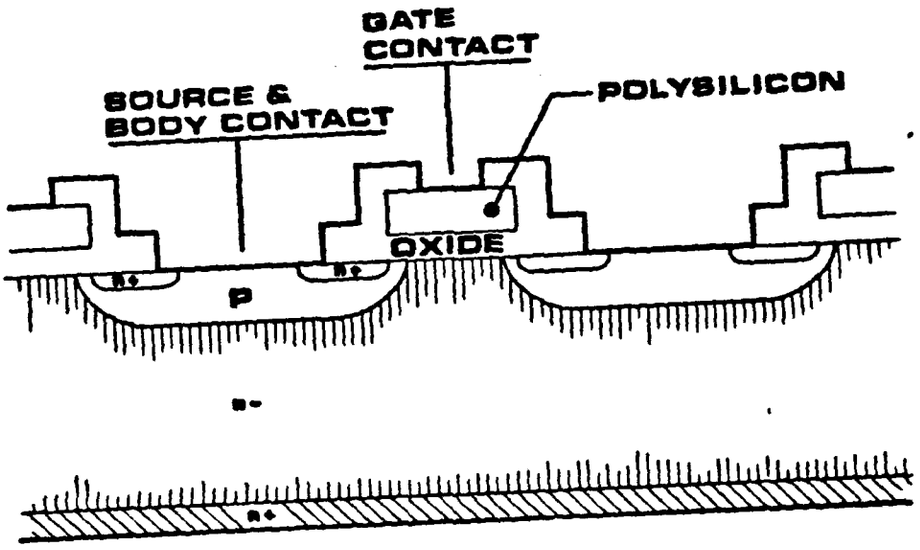


8) Metal formation

-Silicide

-Metal deposition

-Mask 6 - metal definition

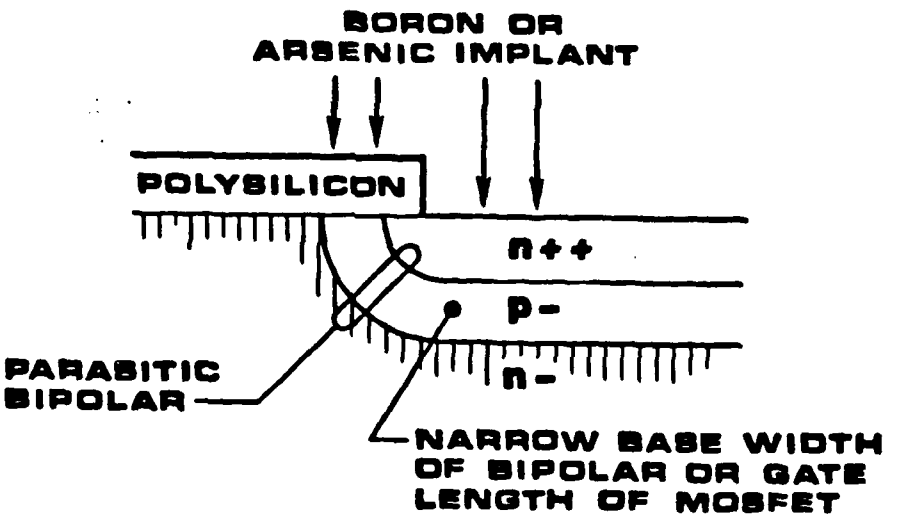


9) Passivation

-Low temperature nitride

-Mask 7 - passivation

It is very important to stress that by forming the gate with this structure, the gate length can be made smaller by increasing the size of the nitride overhand. However, the depth of the boron diffusion can remain constant thereby maintaining a low beta parasitic bipolar device. Typically, had both diffusions originated from the same polysilicon edge, the diffusions would be conformal and creating a smaller channel length that would result in a narrow n+ to P- region forming a parasitic bipolar with a small base width or high beta and high P- buried layer resistance in series with the base as shown below.



2.1.4.1 Epitaxial Variations and Techniques

Besides normal epitaxial resistivity and thickness variations, PHI experimented with variations in graded and

buffered epi. Although an MOS device is a majority carrier device, since a parasitic bipolar transistor exists within the structure, normal bipolar issues regarding reversed biased secondary breakdown apply.

During reverse biased secondary breakdown, caused for instance by severe load mismatch, a current injection mechanism starts from the drain (collector) side of the parasitic bipolar device during forward injection from the source (emitter) side of the bipolar device. This condition of excessively increasing dissipation could destroy the device without typical increased drain ballasting. The traditional design approach for avoiding this problem has been to determine epitaxial thickness needed to sustain the peak drain voltage, then roughly double it. The resistance of the additional silicon provides ruggedness at the expense of output power.

To obtain a solution to this problem, it is necessary to work from a better understanding of the destruction mechanism during excessive current flow.

Figure 2.1.7 shows electric field increasing with increasing current, and illustrates movement of its peak towards the substrate-epi interface. Substrates are normally degenerate semiconductors (doped heavily at 0.003 ohm-cm) and cannot sustain this increasing electric field. The electric field collapses and causes the current to increase out of control. This will result in instant destruction of the device.

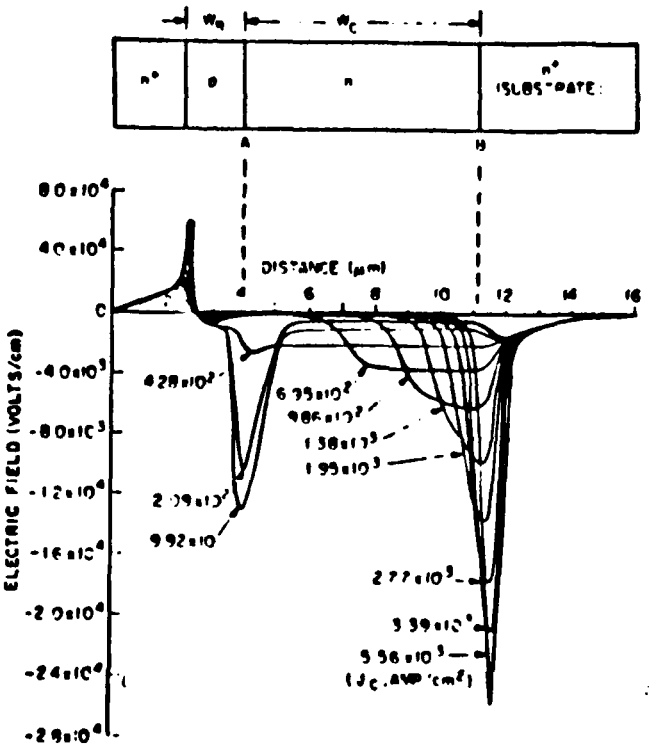


FIGURE 2.1-7 W_B = BASE WIDTH,
W_C = COLLECTOR THICKNESS.
AFTER SZE, PAGE 286.

FIELD STRENGTH VS EPITAXIAL RESISTIVITY AND DISTANCE

In order to sustain this electric field at the epi-substrate interface, a buffered epi region (see Figure 2.1-8) can be introduced which lowers the net field strength. This region may have either a constant but lower resistivity (double epi) or a graded resistivity (graded epi) separating the epitaxial region from the substrate region. PHI has employed both types of epi in addition to standard flat epi in order to improve output power performance while maintaining ruggedness.

2.1.4.2 Double Level Metal

Performance requirements forced additional reductions in input and output capacitances which were obtained by increasing the oxide thickness below the bonding pads. Figure 2.1-9 illustrates the concept of double level metal. Since the finger geometries of the die are relatively small, it becomes very difficult to photolithographically define them if the initial field oxide is thickened (thus increasing the distance from the mask to the feature to be defined) in order to reduce the MOS capacitance contribution from the bonding pads. By employing a double level metal scheme it becomes possible to add an extra two microns of oxide to the field, thereby reducing the MOS capacitance by a factor of three without a penalty in photolithography.

The technique involves defining the narrow metal fingers and a feeder bar on the first layer of metal. A thick silox is then deposited and contact holes are defined. The second layer of metal is then deposited which makes

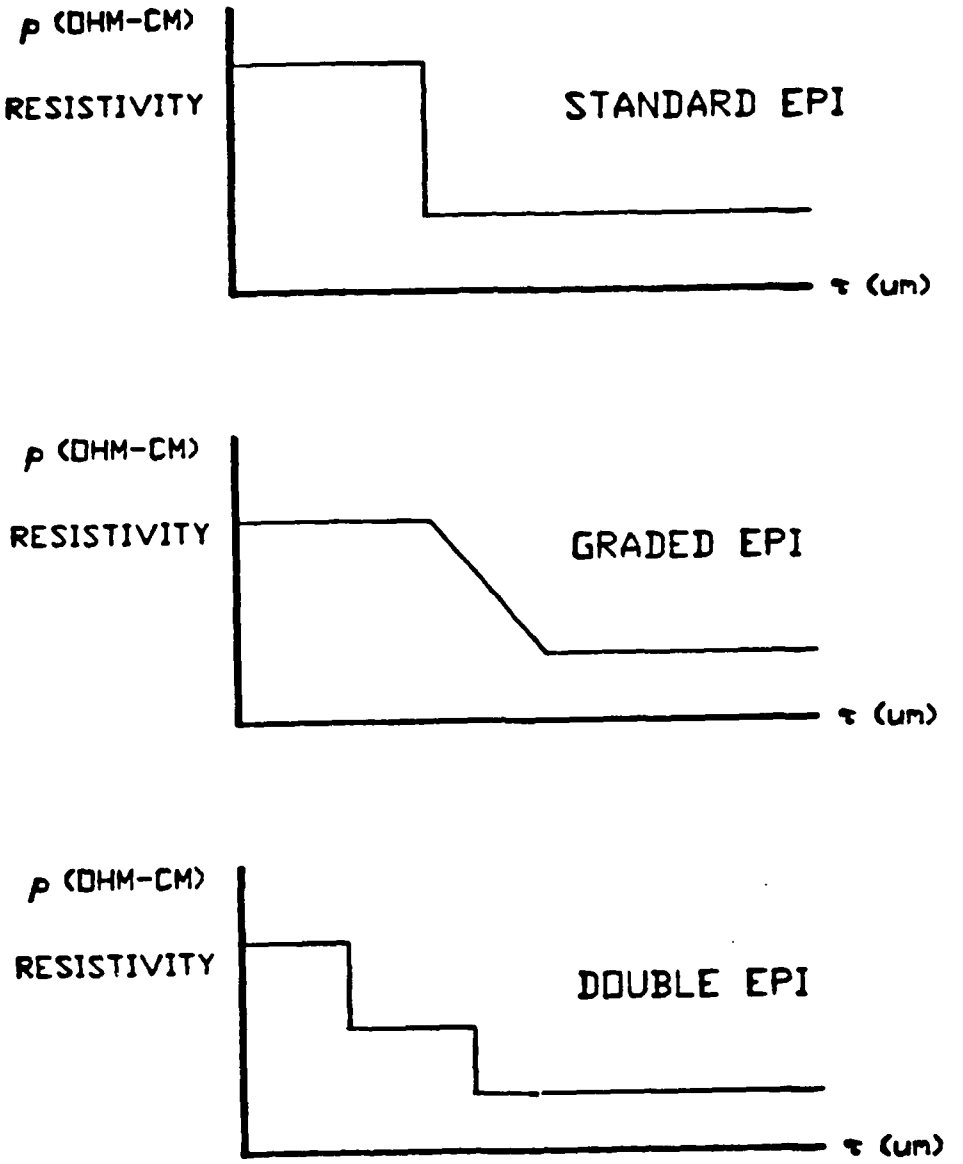
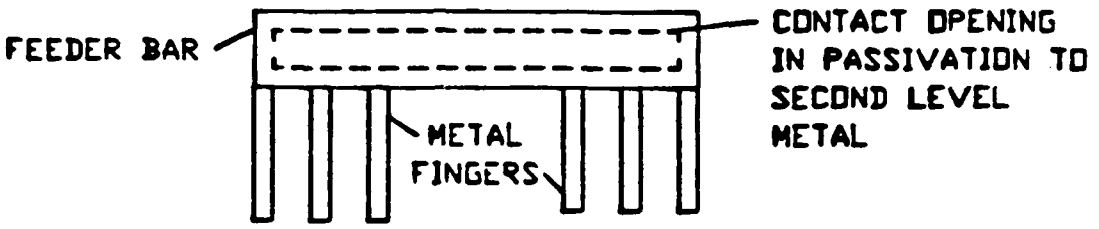
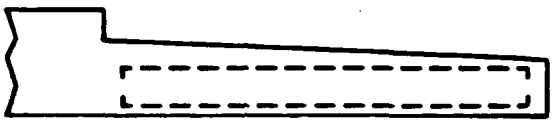


FIGURE 2.1-8 GRAPHICAL ILLUSTRATION OF STANDARD, GRADED, AND DOUBLE EPI. THE LAST TWO ARE ALSO KNOWN AS BUFFERED EPI.



NEW FIRST LEVEL METAL FEEDER BAR



FEEDER BAR WITH SECOND LEVEL METAL

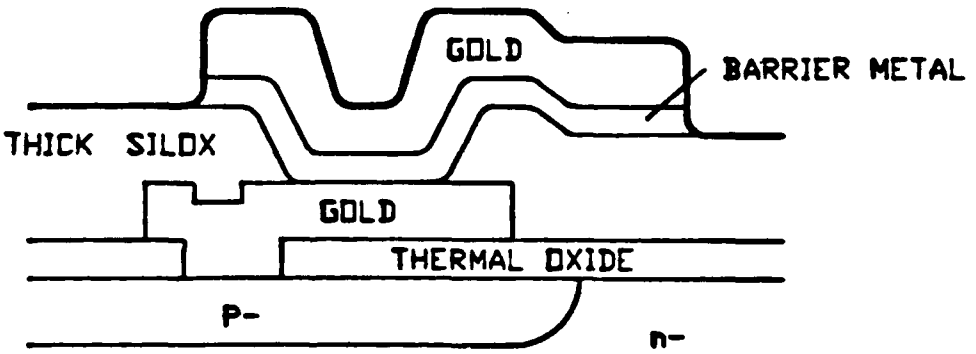


FIGURE 2.1-9 DOUBLE LEVEL METAL CROSS SECTION

contact to the first metal layer and then the bonding pads are defined.

2.1.4.3 C_{rss} Reduction Techniques

As wafer lots were processed and evaluated it became obvious that the feedback capacitance C_{rss} was limiting performance. PHI attempted two C_{rss} reduction techniques, creation of an oxide bump illustrated in Figure 2.1-10 and split poly illustrated in Figure 2.1-11. The oxide plug was difficult to process and was quickly abandoned. The split poly yielded limited performance improvement as noted in Section 2.2, although calculations indicated that the resultant thin poly fingers would present only minor problems with respect to current density issues because of the high inherent gate impedance. It is theorized however that perhaps the C_{rss} reduction gained was offset by gate resistance increases.

2.1.5 Channel Length

Since the f_t of a FET is inversely proportional to the channel length squared, major improvements in gain can be expected as the channel length is decreased. Initial lots had channel lengths on the order of 1.7 microns. Later lots had channel lengths on the order of .9 to 1.0 microns. Attempts to lower the channel length further were relatively unsuccessful because of the polysilicon edge definition and its impact on defining implant edges. Figure 2.1-12 illustrates a polysilicon stripe with perhaps .2-.3 micron occasional edge irregularities. Since the polysilicon edge

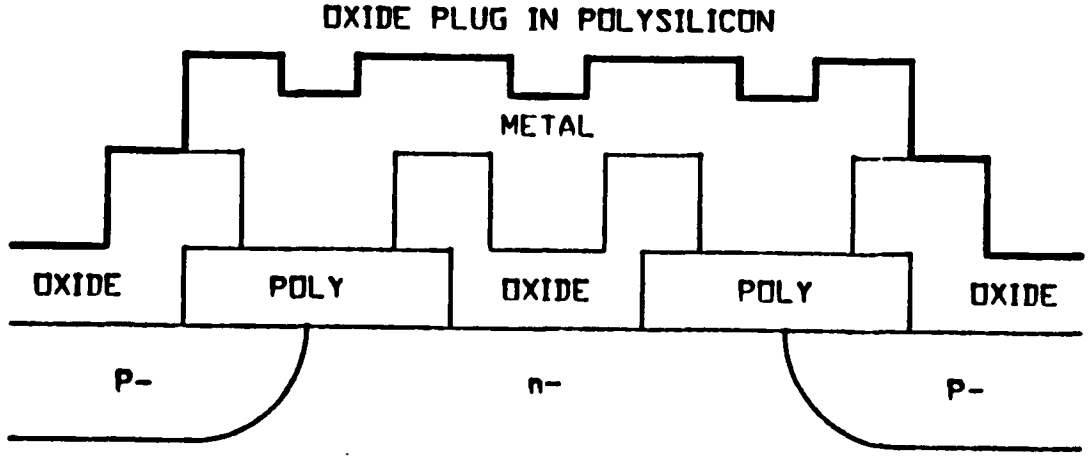


FIGURE 2.1-10 ILLUSTRATION OF OXIDE PLUG IN THE POLYSILICON STRIP

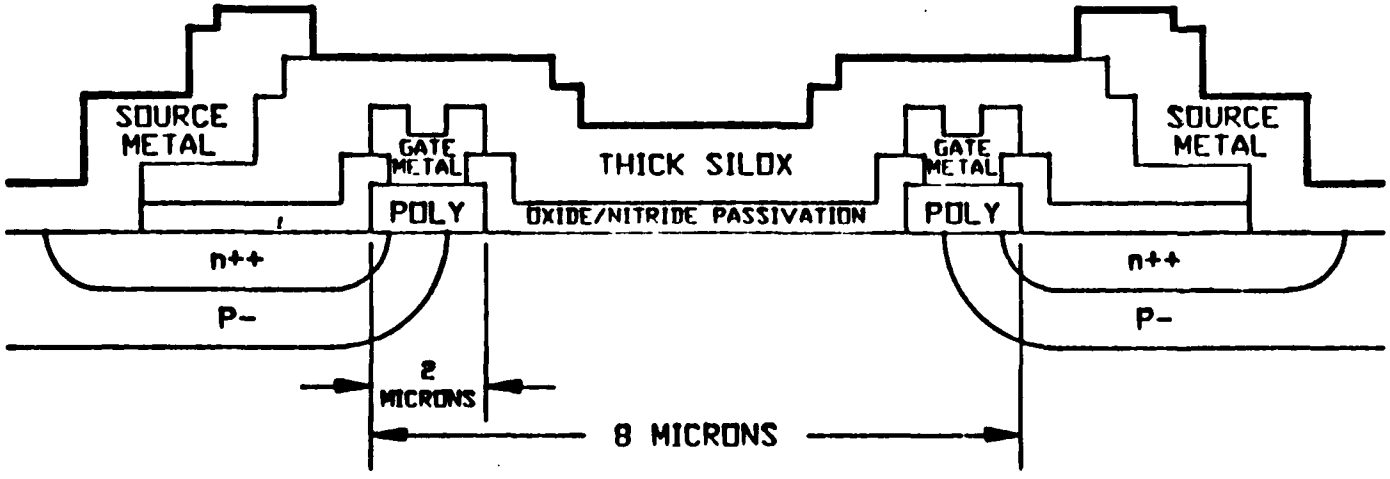


FIGURE 2.1-11 EXAMPLE OF DMOS CROSS SECTION FOR SPLIT POLYSILICON DEVICE

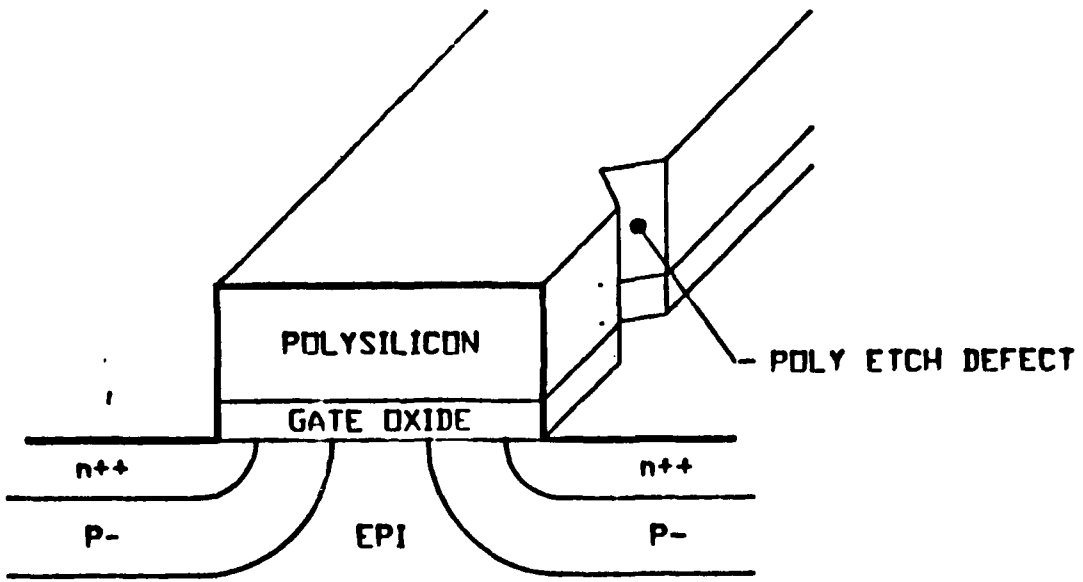


FIGURE 2.1-12 ILLUSTRATION OF POLY ETCH DEFECT CAUSING IRREGULARITY IN CHANNEL LENGTH. POLY EDGE DEFINES IMPLANTS FOR N++ AND P-.

has a great deal of periphery for a power device, it is quite possible to obtain such an irregularity. As shown in Figure 2.1-2 the polysilicon edge defines the implant placement and thus the final diffusion geometry reflects the irregularities. Therefore, a one micron average channel length might have occasional .7 to .8 micron distances. For shorter average channel lengths of perhaps 0.7 microns, the resultant defects might bring the channel length to 0.4 microns at various spots within the die. It became impossible to maintain the breakdown voltage required for 28 volt operation because of depletion within the channel at such spots.

2.2 FET Characterization

2.2.1 ML1 Die Lot Evaluations

A large number of FET die lots were characterized. Most lots were subdivided so that different wafers had different characteristics. In this way, the effects of a large number of variables were evaluated and the performance of the FETs were improved by successive approximation.

Several single cell sample parts were fabricated from each wafer under evaluation. First DC parameters were measured. Breakdown voltages, threshold voltages, transconductance, and on resistance are important parameters that relate to gain, saturated power, efficiency and ruggedness. Small signal S parameters were also measured, and f_T was calculated. The transition frequency f_T is a commonly used figure of merit that describes the high

frequency capability of the transistor. f_T measures small signal current gain and relates to efficiency. The feedback capacitance C_{RSS} does not contribute to f_T but does affect voltage gain and therefore power gain.

The principal RF parameters determined in single cell evaluations are gain, saturated power, and efficiency. Most of these were measured at 1 millisecond 10% duty. Power supply voltage was varied as a parameter because for different lots, optimum performance could occur at different voltages. For each lot the maximum operating voltage was determined either by ruggedness, or by loss of efficiency as voltage increased. Single cell evaluations were primarily made at 1.4 GHz, the upper band edge. 1.4 GHz data at 1 mS, 10%, gives worst case results, and the resulting comparisons between lots and wafers is valid for the entire band.

2.2.2 Single Cell ML1 Evaluations

Four different varieties of the ML1 design were designed into the fabrication mask set to evaluate the effects of finger pitch and cell size. Figure 2.2-1 shows normalized comparison data among the four types. The type 5 cell showed the greatest saturated power, and the greatest number of watts per picofarad, an important parameter relating to broadband capability.

A large number of different ML1 devices were processed for this program. Figure 2.2-2 shows the key material and process parameters of these lots. The single cell test device used for basic die lot evaluation is shown

ML1 DIE TYPES

TYPE	1	2	3	5
Pitch, mils	0.5	0.66	0.86	0.66
Gatewidth, cm	0.33	0.25	0.20	0.35
Active Area, mil^2	39.7	39.7	39.7	55.5
C_{OSG} (1), pF	2.5	2.5	2.4	2.6
P_{SAT} (2), W	2.75	2.63	2.20	3.03
W/cm	8.33	10.52	11.00	8.65
W/pF	1.1	1.05	0.91	1.16

(1) 10E-10, 28V

(2) 10E-10, 28V, 1 mS 10%

Figure 2.2-1 Comparison of Design Parameters of Four Die Variations Evaluated.

LOT/WAFER	ρ·ℓ	METAL PROCESS	SPECIAL PROCESS	CHANNEL LENGTH μm	REMARKS
ML1 1E-3	16.8	Al 1		1.5-1.8	
2E-10	10.0	Al 1		1.0	
5E-8	10.7	Au	Bump	1-1.4	
10E-4	6.6	Al 1	Bump	1-1.2	2u epi reduction
10E-10A	7.2	Al 1	Bump	1-1.2	2u epi reduction
10E-10B	7.2	Al 1	No Bump	1-1.2	
11E-9	5.0	Al 1	Bump	1-1.2	2u epi reduction
11E-21	6.8	Al 2	Bump	1-1.2	2u back diffusion
11E-22	6.8	Al 1	Bump	1-1.2	2u back diffusion
11E-26	8.6	Al 2	Bump	1-1.2	No back diffusion
11E-31	8.0	Al 2	Bump	1-1.2	2u back diffusion
11E-36	6.4	Al 1	Bump	1-1.2	4u back diffusion
11E-41	10.0	Al 1	Bump	1-1.2	No back diffusion
17E-6M 6P	2.8 2.8	Al 1	Split Poly	1-1.2	
17E-20M 20P	3.4 3.4	Al 1	Split Poly	1-1.2	
17E-24M 24P	4.0 4.0	Al 1 Poly	Split Poly	1-1.2	
17E-33M 33P	5.2 5.2	Al 1 Poly	Split Poly	1-1.2	
17E-34M 34P	5.2 5.2	Al 1 Poly	Split Poly	1-1.2	
18E-6	4.0	Al 1	Split Poly	1-1.2	Leaky
18E-8	4.0	Au 1	Split Poly	1-1.2	Leaky
18E-9	4.0	Au 1	Split Poly	1-1.2	Leaky
19E-2	4.0	Au 1	Split Poly	1-1.2	
19E-6	3.3	Au 1	Split Poly	1-1.2	
19E-9	3.3	Au 1	Split Poly	1-1.2	

Figure 2.2-2 Die lot parameters showing special processing and the figure of merit ρ·ℓ.

in Figure 2.2-3. These devices were evaluated as the die lots were completed, and in each case the information gathered was used to determine the targets for the following lots.

Figure 2.2-4 begins a summary of die lot performance. Unlike many bipolar transistors, the power level for optimum operation is not well defined. Gain and efficiency both vary gradually with power level, and when the part is driven to maximize efficiency, the associated gain is low. Similarly, when the part is operated below saturation to improve gain, efficiency is relatively low. The tradeoff between gain and efficiency is more pronounced than with typical L-Band bipolar parts. Experiments with circuit tuning could vary gain and efficiency at a given power level, but did not change the general trend.

To ensure a fair comparison among different wafers, two levels of RF operation are tabulated. Devices are compared at saturated output power, and 1 dB below this point where gain is better. Figure 2.2-5 is a power transfer curve showing the soft gain compression and gradually increasing efficiency of the ML1 as power is increased.

Figure 2.2-4 shows the large improvement in gain, power, and efficiency between the initial lot and lots 10 and 11. A figure of merit, $\rho.\ell$ helps explain the improvement. This is a product of epitaxial resistivity and epitaxial layer thickness. It relates to resistance in series with the drain.

It is evident from Figures 2.2.-1 and 2.2-4 that

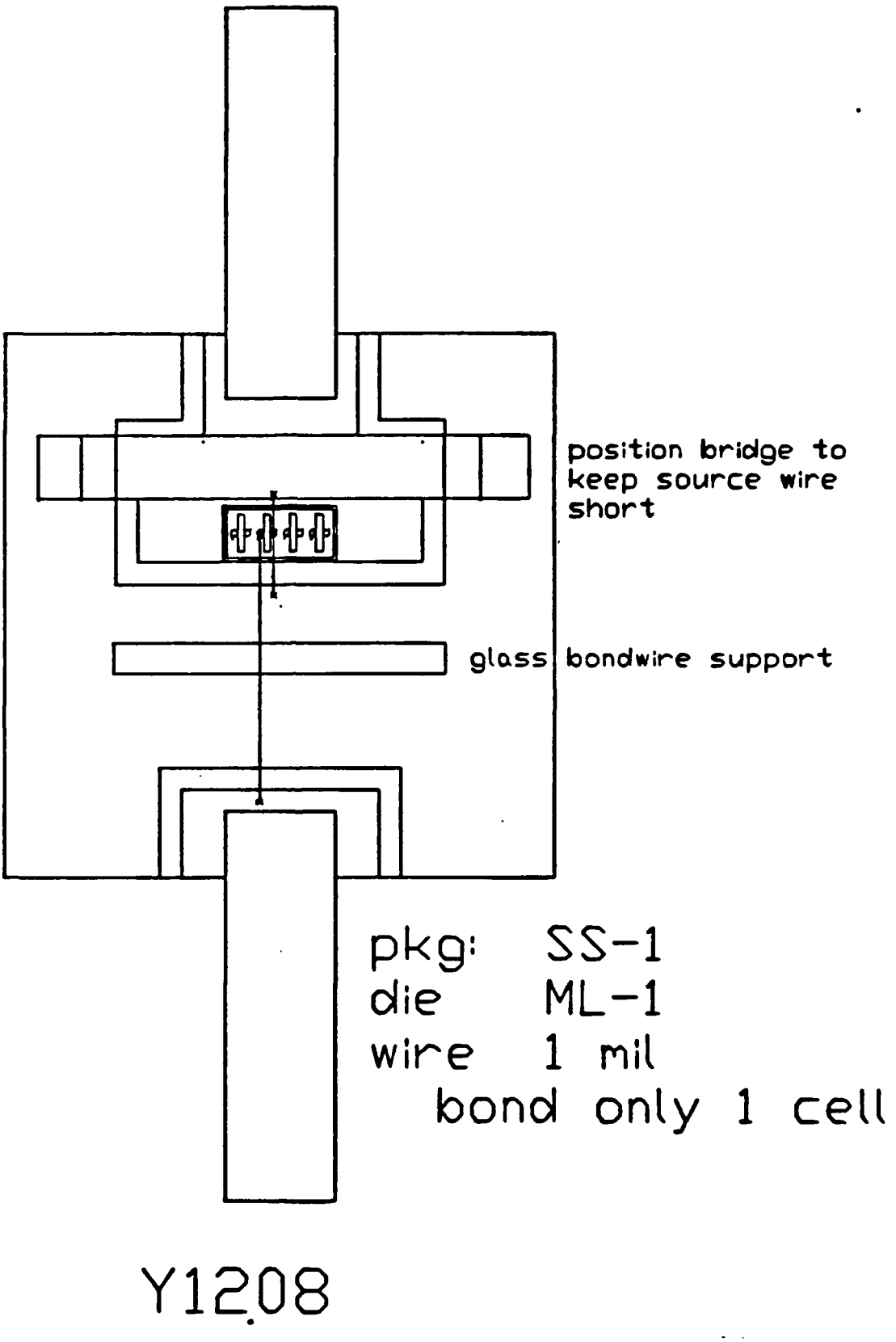


FIGURE 2.2-3. SINGLE CELL TRANSISTOR USED FOR DIE AND PROCESS EVALUATION. MOST EVALUATIONS WERE CARRIED OUT AT 1.4 GHz

LOT/WAFER	TYPE	SAMPLE #	gm max @ Id	Ron ohms	ft MHz	Po W	G dB	n %	Psat W	G dB	n %
ML1 1E-3	2	M132	85@ 120	27	1824	1.16	4.4	39.6	1.48	2.9	44.0
2E-10	2	M133	60 @ 100	12.5	2959	2.0	7.4	44.6	2.55	5.3	52.0
5E-8	2	M141	40@ 130	20	3068	----	----	----	----	----	----
10E-4	2	E5066	60 @ 120	11.8	3658	2.41	9.6	50.6	3.03	6.0	56.0
10E-4	5	E5006	87 @ 200	8.3	3677	3.23	9.7	50.2	4.08	6.9	56.0
10E-10A	2	M157	80 @ 150	12.0	3560	1.83	10.2	39.5	2.37	6.5	43.4
10E-10B	2	E4969	70 @ 218	11.1	3331	1.82	8.3	42.0	2.28	6.3	45.2
11E-9	2	E5177	70 @145	10.0	3300	2.8	9.4	50.0	3.55	6.3	54.6
11E-9	5	E5230	95 @ 210	7.8	3500	3.62	9.8	50.8	4.53	7.4	57.8
11E-21	2	E5101	70 @ 170	11.7	3538	2.22	9.7	51.2	2.8	6.6	51.3
11E-26	2	E5102	64 @ 150	13.3	3295	2.05	9.1	50.5	2.6	6.3	54.6
11E-31	2	E5100	70 @ 175	11.7	3365	2.23	9.7	48.3	2.81	6.6	54.2

Figure 2.2-4 DC and RF Performance of ML1 Lots.
CONDITIONS: f = 1400 MHz
duty 2 ms 20%
V_{cc} 28V
I_{dq} 50mA

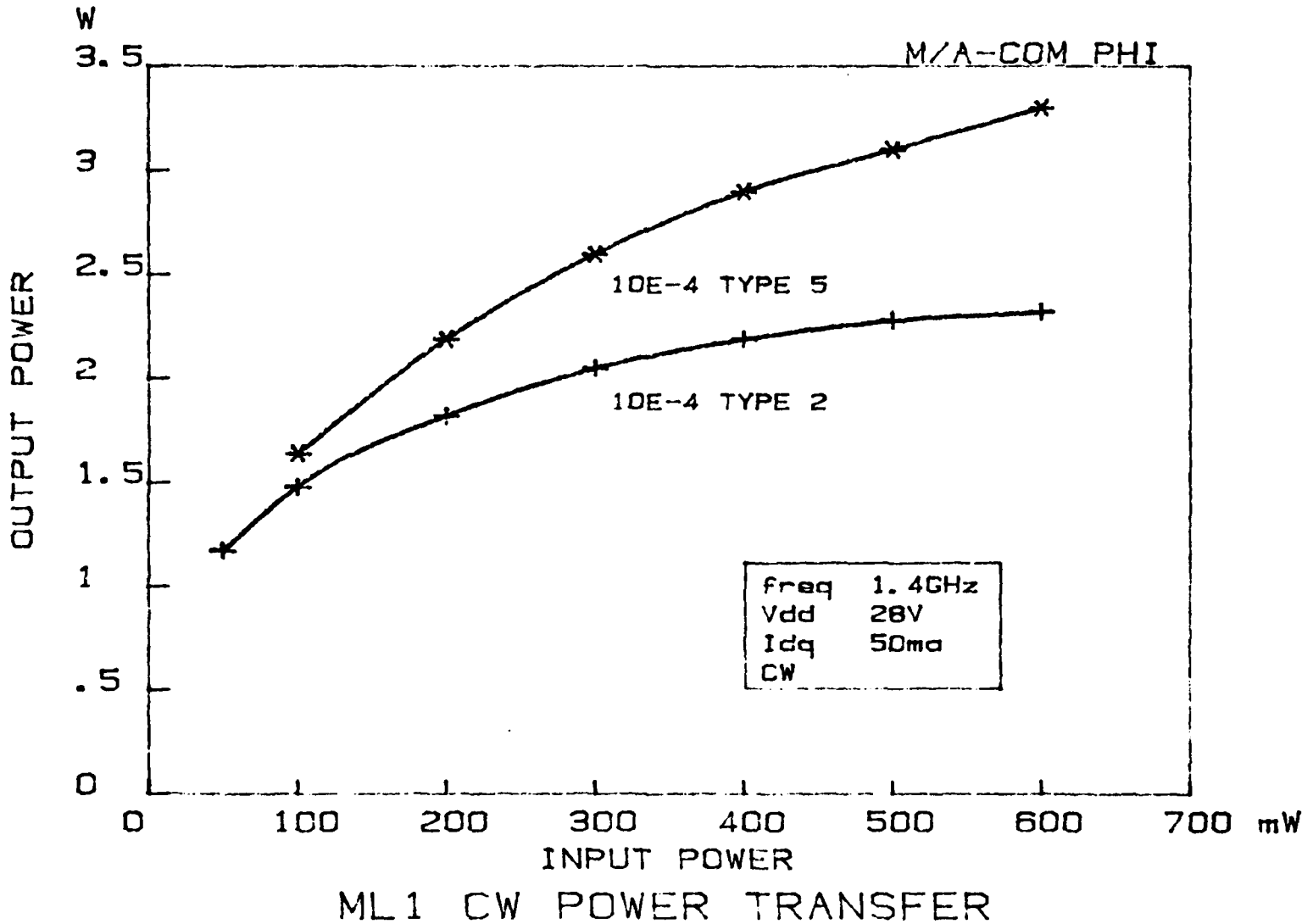


FIGURE 2.2-5 CW ML1 Cell Performance.

the $\rho \cdot \ell$ product is highly correlated with die performance. A low $\rho \cdot \ell$ product is associated with high gain and efficiency. However, as the product is further reduced, die ruggedness will be reduced. The use of a double epitaxial structure or a graded epitaxial layer helps maintain ruggedness as the $\rho \cdot \ell$ product is reduced. Lots 10 and 11, the best performing lots in Figure 2.2-4, have this structure.

Figure 2.2-6 shows measured gain and efficiency as a function of the $\rho \cdot \ell$ product. As the product is reduced from 14 to 6.5, gain and efficiency improve greatly, and ruggedness is still excellent. When operating voltage may be varied and is not limited by ruggedness, saturated output power and efficiency are the primary factors determining the optimum voltage. Figure 2.2-7 shows the voltage-power tradeoff of lot 2 and lot 10 devices. Figure 2.2-8 shows the variation of f_T with voltage and current. All devices through lot 10 were operated at 28V. Some of the later devices with lower $\rho \cdot \ell$ products required lower operating voltages. In these devices, the loss in performance due to lower operating voltage outweighed the advantage of the reduced $\rho \cdot \ell$ product.

As we gained experience with the ML1, we progressively reduced the channel length. The transition frequency f_T is a strong function of channel length. Its progressive increase with reduced channel length is shown in Figure 2.2-8b.

PERFORMANCE VS. EPI FIGURE OF MERIT

EPI RESISTIVITY X EPI THICKNESS
(OHM-CM) (MICRONS)
TYPE-2

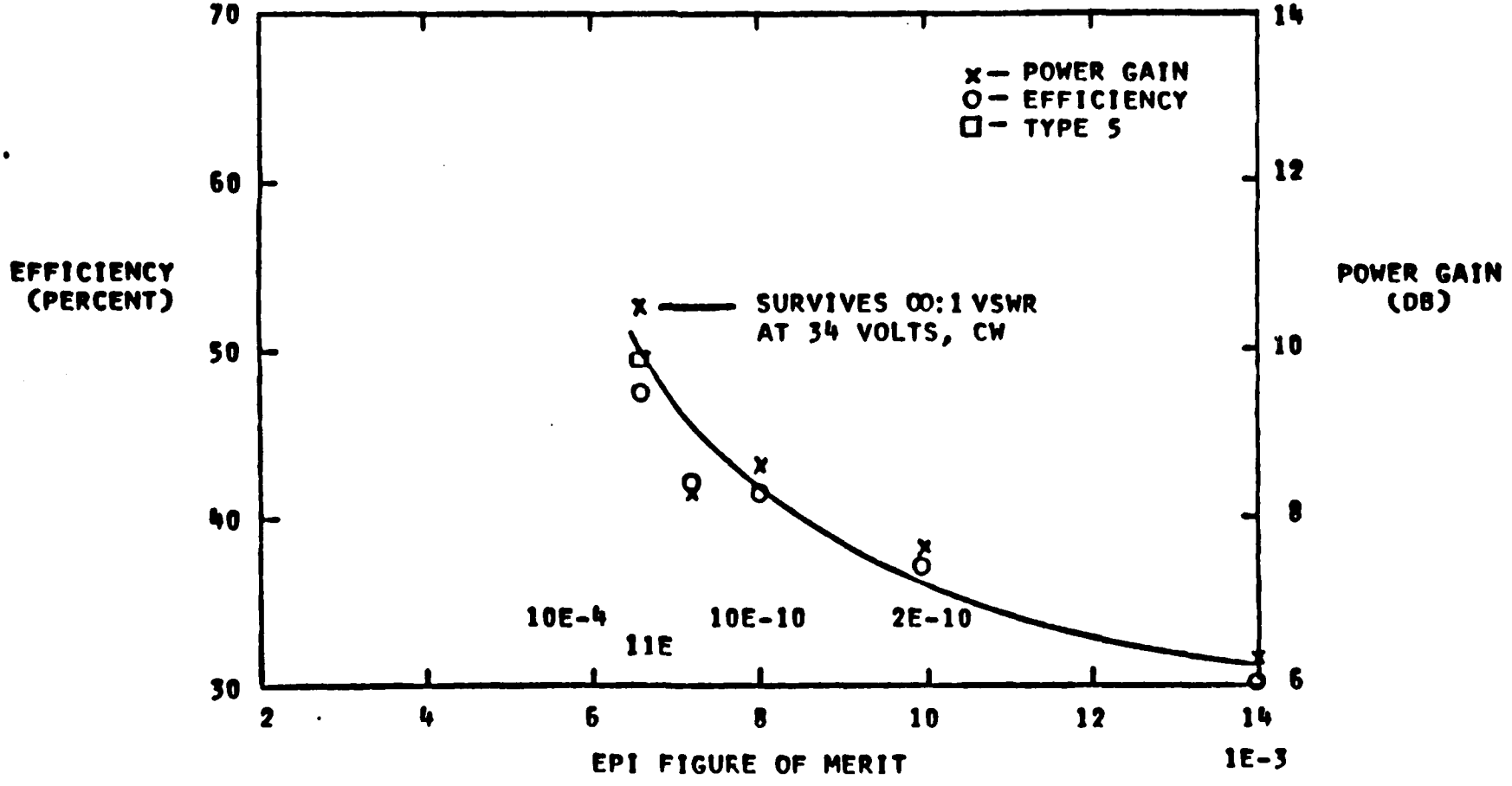


Figure 2.2-6

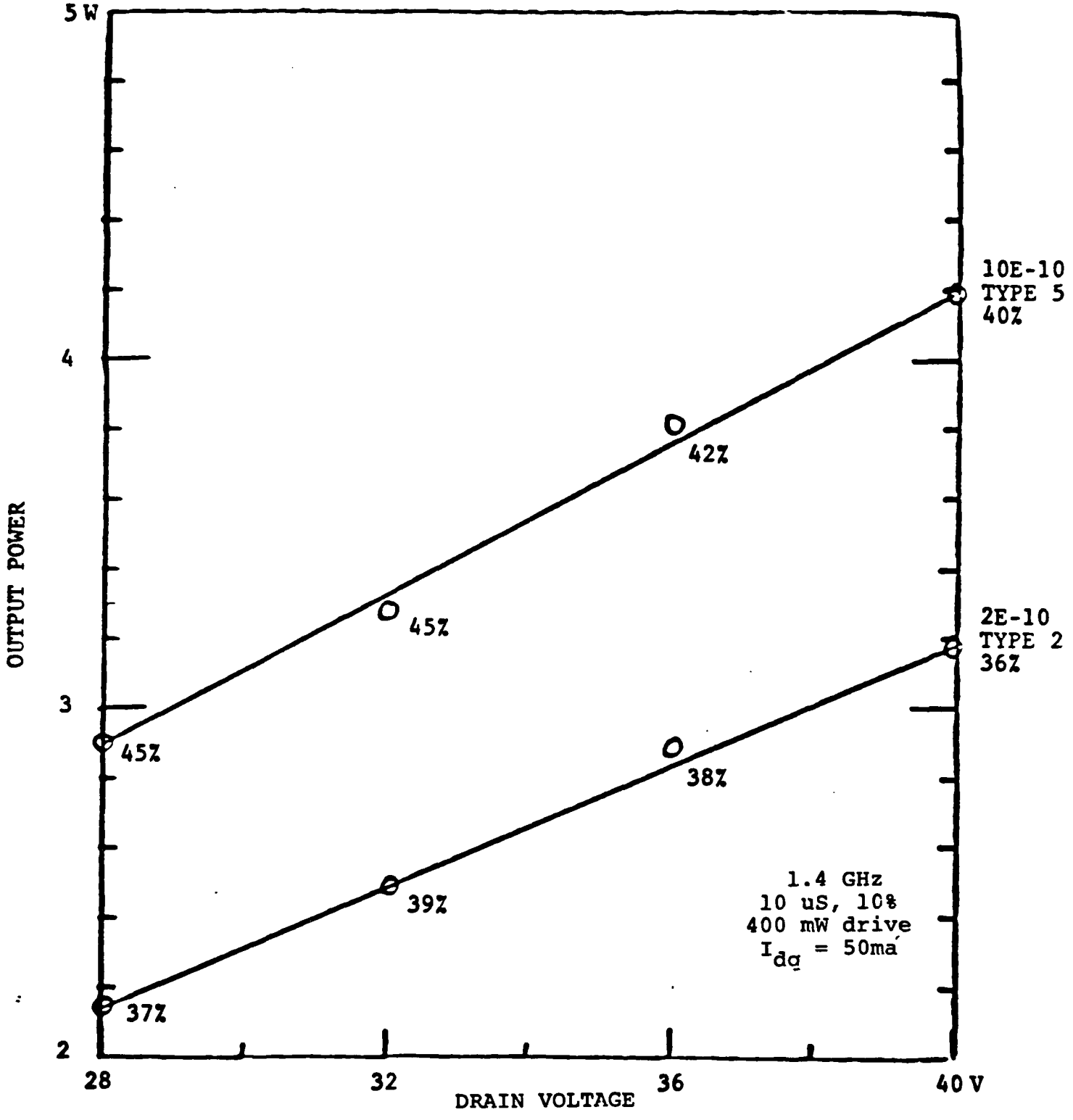


Figure 2.2-7a **ML1 Cell Performance Vs. Voltage.**
Drain efficiency is noted at each data point

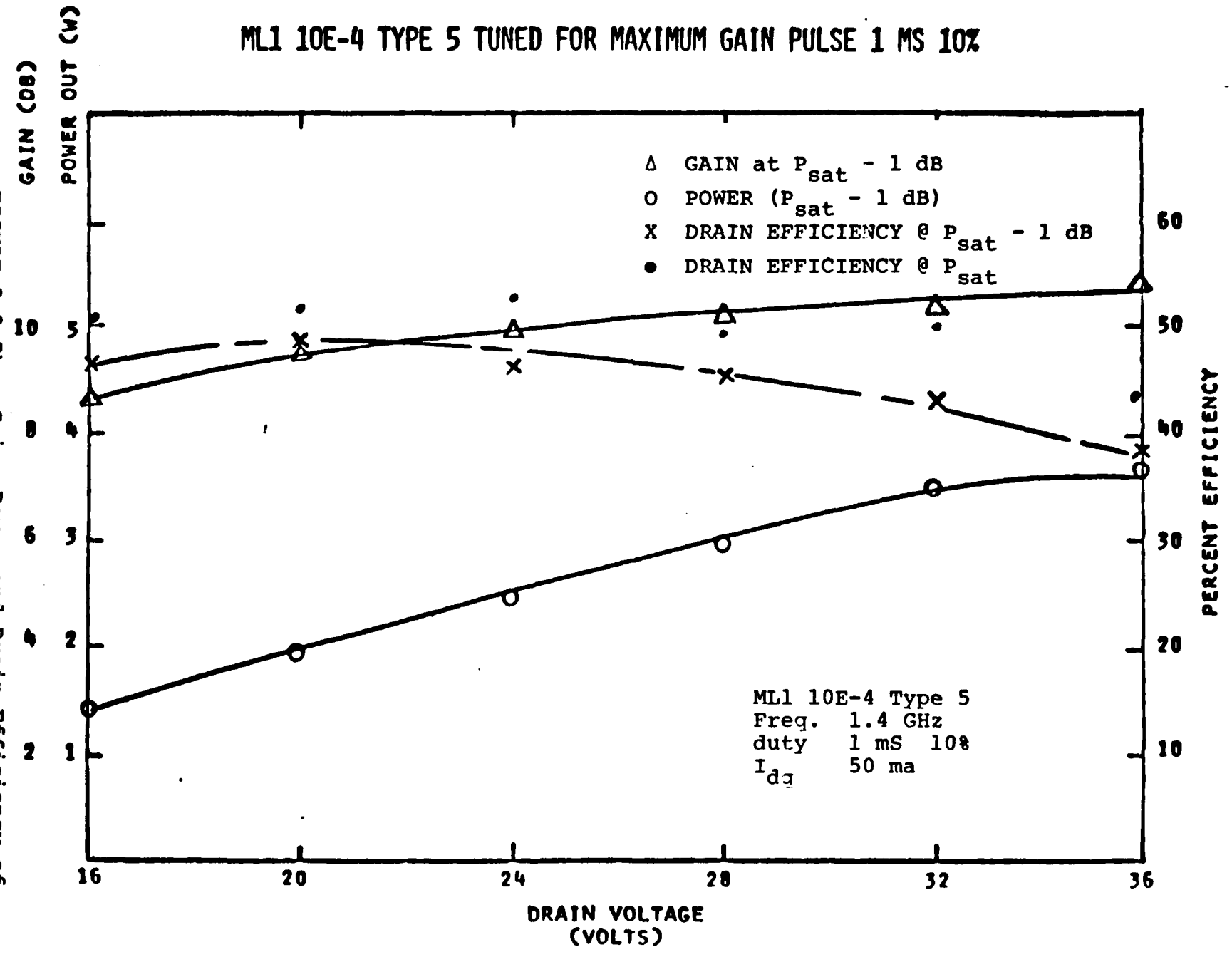
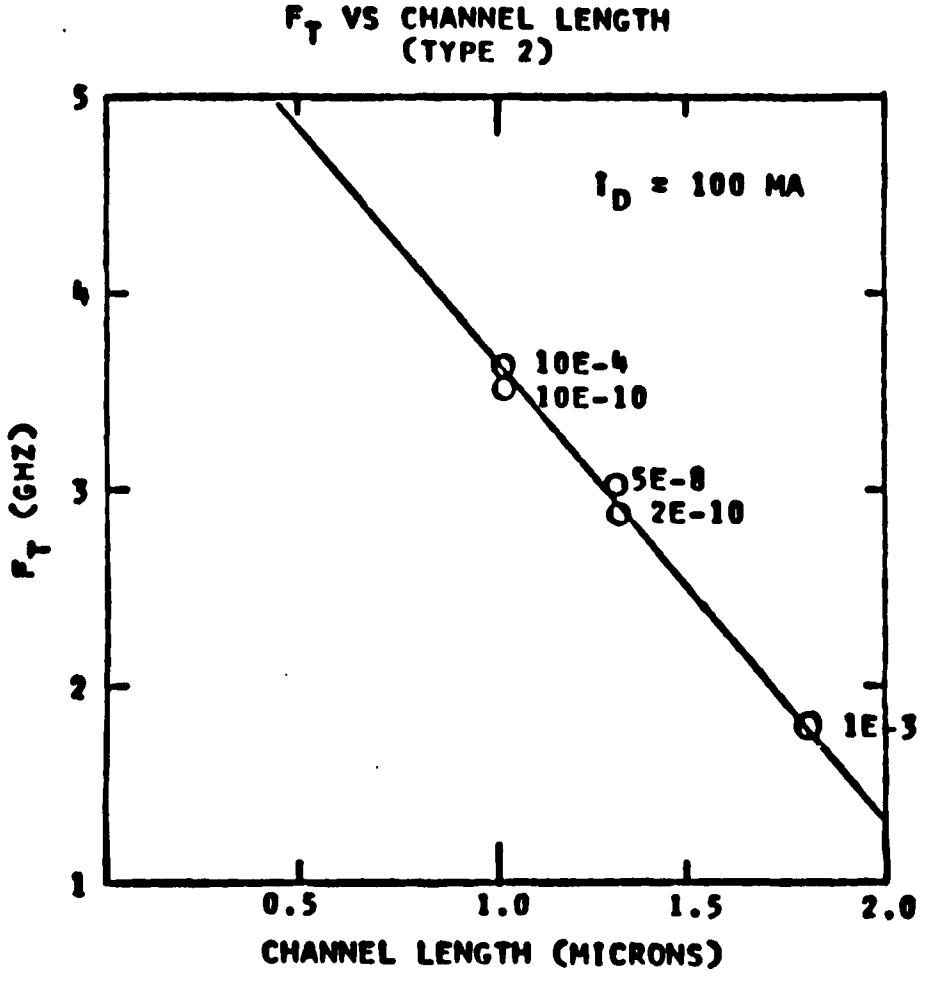


FIGURE 2.2-7b. Gain, Power and Drain Efficiency of ML1 die vs drain voltage

f_T VS. BIAS

V	I	11E-9 TYPE 5	11E-9 TYPE 2
36V	50mA	3843	3670
	71	3942	3675
	100	4000	3612
28V	50	4000	3778
	71	4050	3759
	100	3960	3550
	141	3800	3220
	200	3440	2211
20V	50	4010	3710
	71	4109	3715
	100	4152	3725
	141	4000	3535
	200	3734	3100
	280	3130	2150

Figure 2.2-8 f_T of ML1 Die vs. Voltage and Current; f_{MEAS} = 1.3 GHz



NOTE:

F_T = 3.9 GHZ
TYPE 5
I_D = 100 MA

PREDICTION:

F_T = 5.5 GHZ
TYPE 5
.7 MICRONS

Figure 2.2-8b Measured f_T vs. Channel Length for ML1 FETs.

Figure 2.2-9a shows DC and small signal characteristics of lots 17 through 19. Here also, $\rho.\ell$ is clearly a significant parameter. However, in these lots the epitaxial material was reduced to the point that ruggedness was a factor. Figure 2.2-9b shows RF performance, including ruggedness, of these dice. For these dice, operating voltage was limited by ruggedness, so comparing wafers at a constant operating voltage is not correct. Rather, each die type was operated at the highest voltage at which that particular die had acceptable VSWR tolerance.

Other changes were also evaluated using these devices. Lot 5 and later lots use an additional masking step to increase oxide thickness above the drain and thereby reduce parasitic capacitance. Some of the observed performance improvement is due to this reduction. Wafer 10E-10 contained devices with and without the thick oxide. In Figure 2.2-4 the 10E-10A devices have the thick oxide, the 10E-10B devices do not.

A double level metal process (DLM) was also introduced to reduce parasitic MOS capacitance by increasing the oxide thickness under bonding pads. Figure 2.2-10 shows a one-half dB difference in gain and power between two wafers that are identical except for the reduced capacitance.

The split-poly process, described in Section 2.1, reduces the feedback capacitance by eliminating a portion of the gate fingers that overlay the drain. Figures 2.2-11 and 2.2-12 show that the process successfully reduced the

LOT/WAFER	SAMPLE #	BVdss V	gm max @ Id mS ma	Ron Ohms	Cisg pF	Crss pF	Cosg pF	ft MHz	MAG dB	Rl ohm cm
17E-6 M	E5650	55	105 @ 260	4.9	2.5	.70	3.0	4684	14.4	2.8
P	E5649	45-55	105 @ 270	4.8	2.5	.65	1.5-3.0			
17E-20 M	E5652	52-59	100 @ 280	5.6	2.5	.57	2.9	4716	19.7	3.4
P	E5651	55	100 @ 290	5.6	2.5	.60	2.9			
17E-24 M	E5663	51-56	108 @ 260	5.9	2.5	.57	2.9	4877	16.9	4.0
P	E5664	50	105 @ 360	5.6	2.5	.60	3.3			
17E-33 M	E5666	60	97 @ 260	8.7	2.6	.50	2.9	4191	20.6	5.2
P	E5665	60	100 @ 270	8.9	2.6	.45	3.0	4011	16.9	5.2
17E-34 M	E5668	61	80 @ 200	10.0	--	.44	--	4638	27.2	5.2
P	E5667	62	80 @ 200	10.0	--		--	4346	20.4	5.2

Figure 2.2-9a. D.C. and Capacitance Characteristics of Split-Poly Type ML1 FETs

LOT/WAFER	SAMPLE #	Vdd V	Pc W	G dB	n %	Psat W	G dB	n %	VSWR
17E-6 M	E5651	20	3.08	8.9	44.6	3.9	6.7	50.7	Pass 3:1, Fail 4.4:1
		24	3.7	8.7	42.4	4.6	6.3	43.1	
		28	4.7	7.9	45.1	6.0	5.6	44.2	
17E-6 P	E5649	20	2.8	8.2	44.3	3.5	6.7	51.0	Pass 4.4:1, Fail 8.6:1
		24	3.9	7.6	47.6	5.0	5.8	51.7	
		28	Not measured						
17E-20 M	E5652	20	2.6	10.4	52.7	3.3	8.4	56.3	Pass 8.6:1
		24	3.5	10.0	35.3	4.5	8.0	46.2	Fail 3:1
		28	Not measured						
17E-20 P	E5651	20	2.4	8.0	48.8	3.0	6.2	52.8	Pass 8.6:1
		24	2.9	8.7	43.5	3.6	7.3	49.4	Fail 3:1
		28	Not measured						
17E-24 M	E5663	20	2.7	9.0	43.0	3.4	6.6	43.4	Pass 8.6:1
		24	3.7	8.8	47.3	4.6	6.3	52.6	Fail 3:1
		28	4.1	9.2	43.1	5.2	7.2	48.5	Fail 3:1
17E-24 P	E5664	20	2.3	7.8	39.2	2.9	5.9	42.8	Pass 8.6:1
		24	3.1	6.8	44.0	3.9	3.4	52.0	Fail 3:1
		28	Failed			Failed			
17E-33 M	E5666	20	1.7	7.7	47.5	2.2	5.3	49.9	Pass 8.6:1
		24	Not measured						Fail 3:1
		28	Not measured						
17E-33 P	E5665	20	1.5	6.8	40.0	1.9	5.2	46.4	Pass 8.6:1
		24	1.91	6.8	45.0	2.4	5.1	46.8	Fail 3:1
		28	2.3	7.2	41.0	2.9	5.5	46.5	Fail 3:1

Figure 2.2-9b RF Performance and Ruggedness of Split-Poly Type ML1 FETs.

LOT/WAFER	SAMPLE #	Vdd	Pc W	G dB	n %	Psat W	G dB	n %	VSWR
17E-34 M	E5668	20	1.7	8.7	43.3	2.15	6.3	47.8	Pass 8.6:1
		24	Not measured---			2.6	7.2	46.7	Pass 3:1, Fail 4.4:1
		28	2.7	10.2	40.8	3.4	7.7	46.1	
17E-34 P	E5667	20	1.4	7.3	38.3	1.8	5.6	41.8	Pass 8.6:1
		24	Not measured ----------						
		28	2.2	8.1	39.7	2.9	6.4	43.6	Pass 3:1, Fail 4.4:1

Figure 2.2-9 b(Continued)

LOT/WAFER	DUTY CYCLE		SATURATION			1dB BELOW Psat			
			Po W	G dB	n %	Po W	G dB	n %	
10E-4 TYPE 5	2ms	20%	4.08	6.9	56.8	3.23	9.7	50.2	
11E-9 TYPE 5	2ms	20%	4.53	7.4	57.8	3.62	9.8	50.8	(a)
11E-22 TYPE 2 (SLM)	1ms	10%	2.55	6.2	52.0	2.02	8.9	49.8	
11E-21 TYPE 2 (DLM)	1ms	10%	2.80	6.6	51.3	2.22	9.7	51.2	(b)

Figure 2.2-10 Comparison of Single-Cell Performance of ML1 Dice

(a) Two best performing wafers. $\rho.\ell$ is 6.6 for 10E-4 and 5.0 for 11E-9.
(b) Single level metal vs. double level metal. Both wafers have a $\rho.\ell$ of product of 6.8.

Drain Voltage: 28V

Quiescent Current: 5mA

Frequency: 1.4 GHz

SAMPLE	LOT/WAFER	TYPE	METAL OVER GATE	BV_{dss} V	G_m mS	R_{on} OHM	fT MHz	Crss pF
E5310	11E-9	3	Y	68	56	13	3700	.525
E5311	18E-8	3	N	55	60	9.5	Not Measured	
E5312	18E-8	3	Y	28-64	57	13	4100	.252
E5308	18E-9	3	Y	54	60	13	4100	.314
E5304	18E-9	1	Y	32-36	90	10	3900	.407

Figure 2.2-11 Comparison of several ML1 dice with split-poly processing to the best performing standard ML1, (11E-9).

SAMPLE	LOT/WAFER	TYPE	METAL OVER GATE	SATURATION P W	SATURATION G dB	SATURATION n %	1 dB BELOW SATURATION P W	1 dB BELOW SATURATION G dB	1 dB BELOW SATURATION n %
E5310	11E-9	3	Y	2.75	7.2	55.0	2.20	10.6	46.0
E5311	18E-8	3	N	2.37	6.9	45.8	1.80	8.9	34.9
E5312	18E-8	3	Y	2.55	8.3	49.2	2.04	11.3	41.6
E5308	18E-9	3	Y	2.40	7.8	51.9	1.91	11.7	50.7
E5309	18E-9	1	Y	3.09	8.3	51.9	2.48	11.3	45.4

Figure 2.2-12 RF Performance of Split-Poly ML1 Devices vs Standard Device (11E-9).

F=1.4 GHz
Vdd=28V
Duty=2mS, 20%

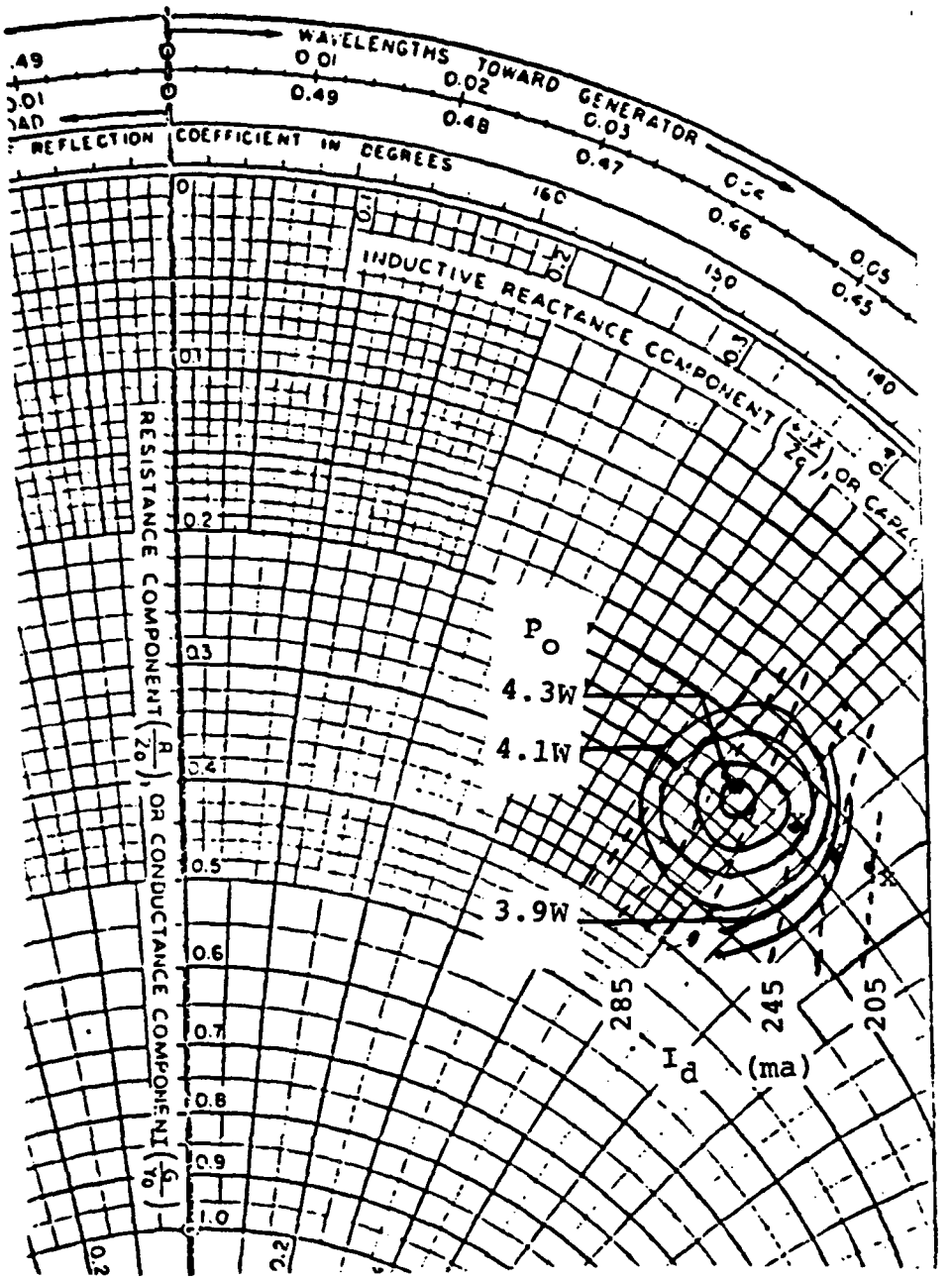
feedback capacitance C_{RSS} and improved f_T, but the improved small signal performance did not result in improved saturated power and efficiency.

Comparison of the different wafers shows that none have a significant advantage in power, gain, and efficiency over wafers 10E-4 and 11E-9. These wafers, with a double-epitaxial structure and standard polysilicon processing, are rugged up to 34V, but have reduced efficiency above 28V.

Figure 2.2-13 shows load pull data for one of the best 11E-9 devices measured. The closed curves are contours of constant power while the nearly straight lines are constant drain current contours. Optimum power occurs at the center of the smallest circle, but operation at that load impedance does not correspond to maximum efficiency. Moving circuit impedance along the power/efficiency tradeoff line will improve efficiency at minimum cost in gain. The performance tabulated in the inset therefore represents the best narrowband performance obtained with ML1 die. This performance is sufficient to meet the contract goals.

2.2.3 Four Cell ML1 Results

The single cell narrowband measurements discussed in the preceding section served to compare dice with different material and processing. The output impedance of these FETs was similar to that of a comparable bipolar die. However, their input impedance and its variation with frequency are substantially different from those of bipolar transistors.



GAIN/EFFICIENCY TRADEOFF

Power W	Eff %	Gain dB
4.3	55.8	8.3
4.15	60.5	8.1
3.83	60.8	7.8
3.63	63.2	7.5

———— Const Power Contours

------- Const Current Lines

x Power vs. Efficiency Tradeoff

Z_o = 50 ohm

FIGURE 2.2-13. ML1 Load Pull Data Showing Tradeoff Between Saturated Power and Efficiency

Impedance matching requirements and broadband capability were investigated using four cell devices. A four cell ML1 device with internal input and output matching provided over 10W across the 1.2-1.4 GHz band using a 2 mS, 20% pulse. Figure 2.2-14 shows the performance obtained. The output match was a conventional internal shunt L. However, conventional low-pass L-C matching sections were not appropriate for the input match.

Die input impedance was difficult to measure because of the high Q and low real part of the impedance. Reproducibility of the results was poor. However, all measured results clearly showed that the input impedance was highly capacitive, with a Q of 8 to 16. The real input impedance was near 1 ohm, a value comparable to that of a bipolar transistor. The large capacitive component meant that conventional internal input matching was ineffective. The internal shunt L shown in Figure 2.2-15 solved the matching problem and provided a mid-band input impedance near 7 ohms. This approach worked well over the full TPS-59 bandwidth, and was achieved in a conventional microwave transistor package.

2.2.4 DMOS Limitations

One of the important factors in ML1 performance was efficiency. During development, the ML1 DMOS structure was improved considerably by gate length reduction, split-poly processing, double level metallization, a lightly doped source process, and careful optimization of the epitaxial

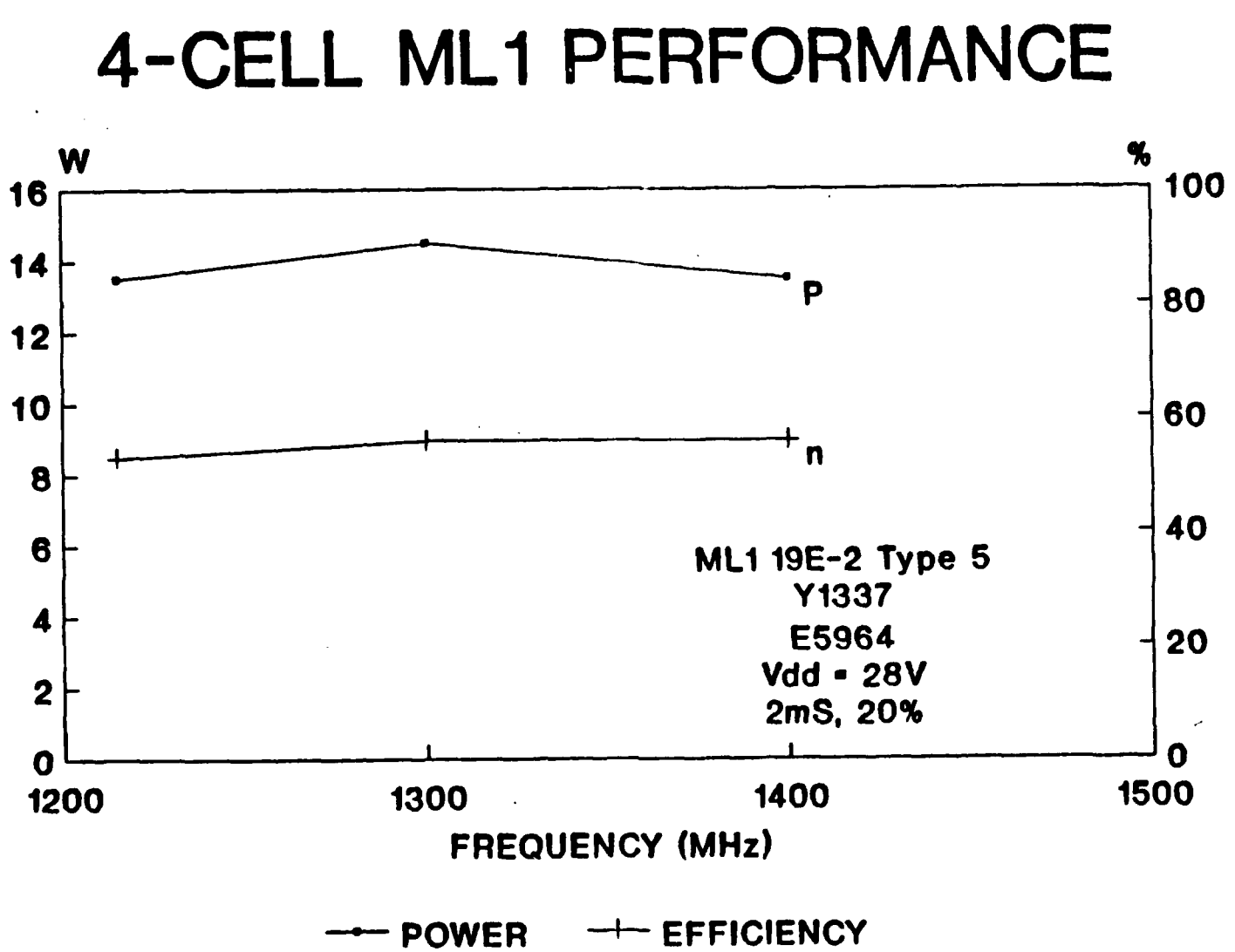


Figure 2.2-14a **Performance Comparison of 4-Cell ML1 FETs** from wafers with different processing. Power output and drain efficiency with 2.5W drive are shown.

(a) Wafer ML1 19E-2; Gold Metallized, with Split Poly Process

4-CELL ML1 PERFORMANCE

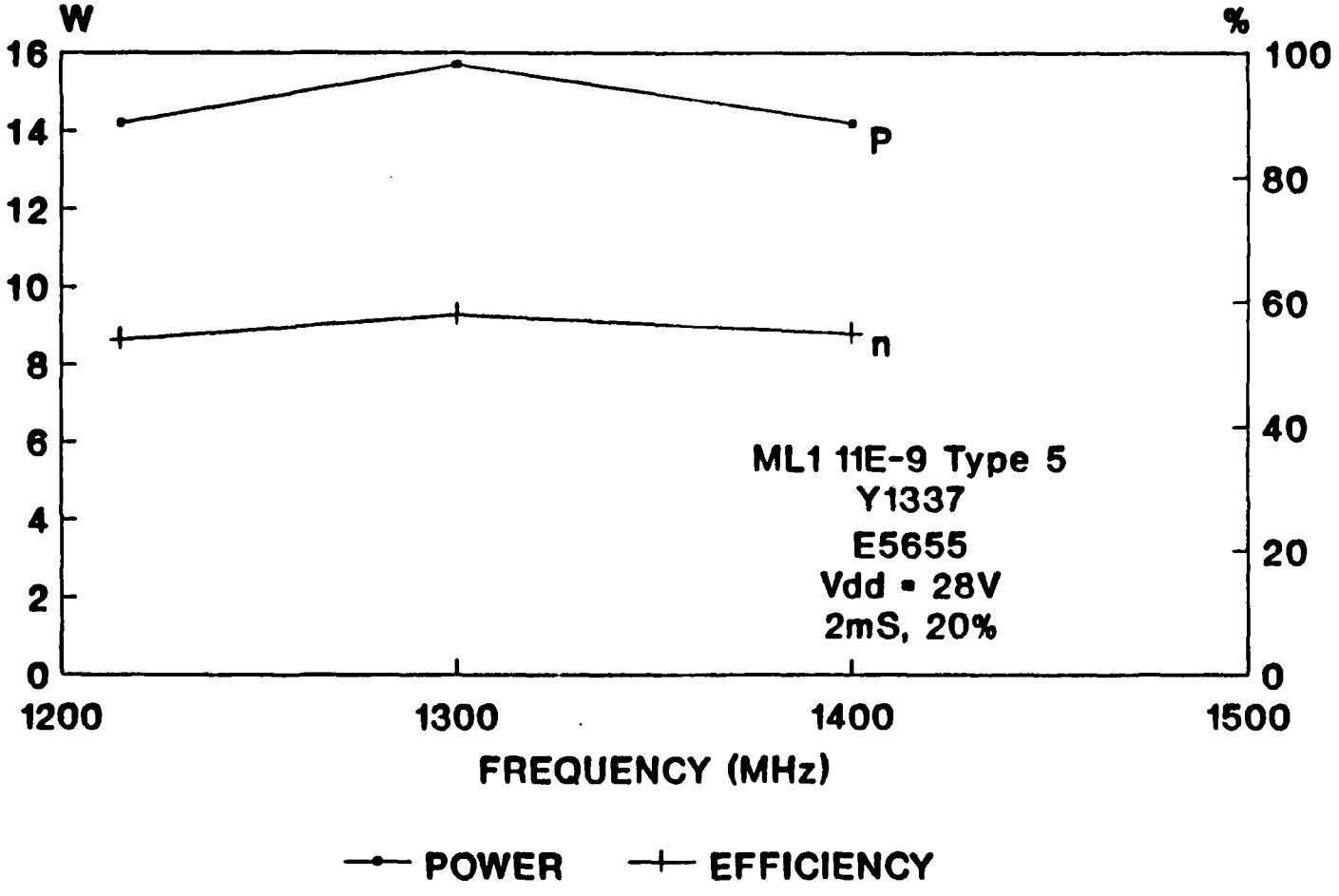
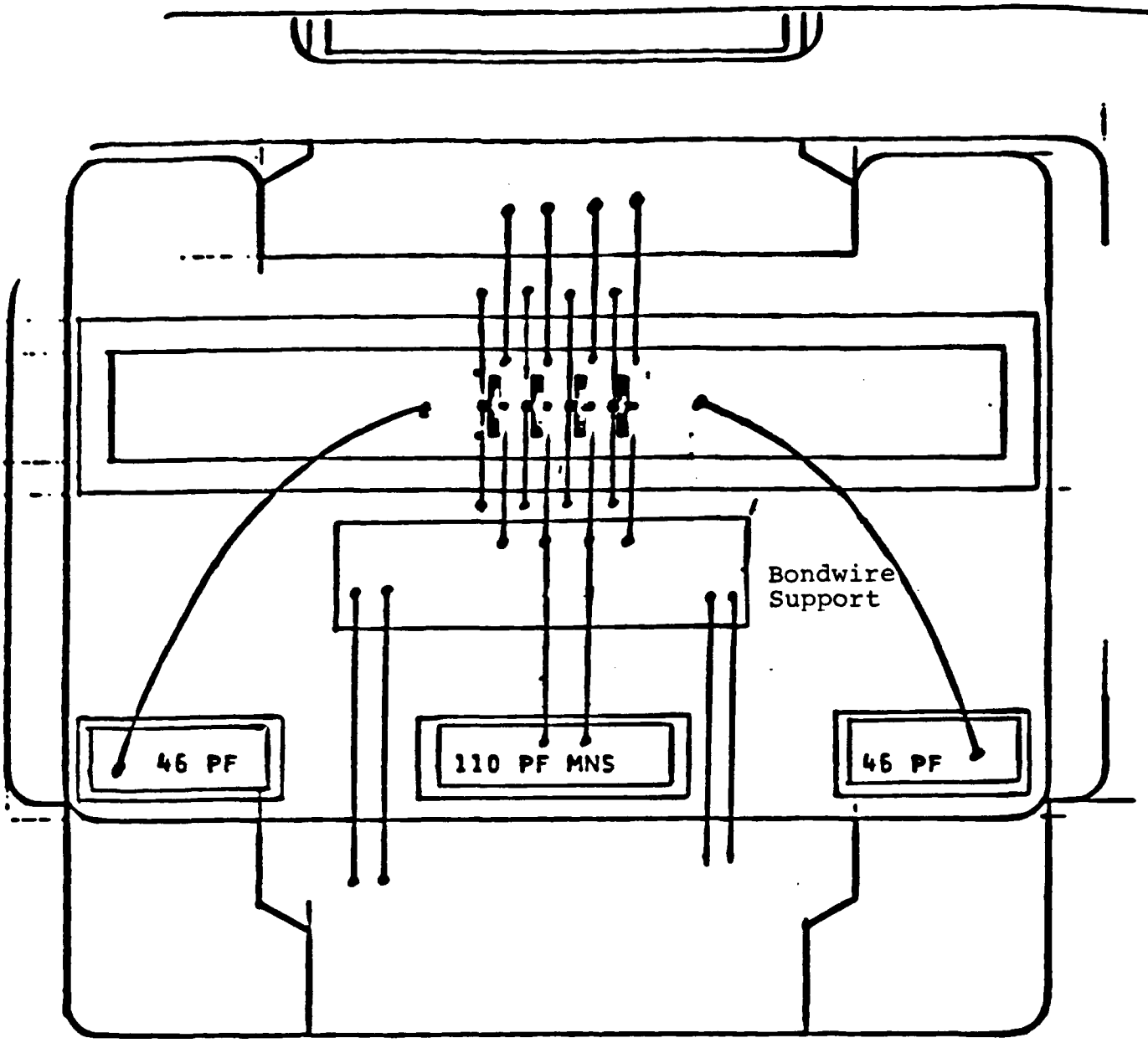


Figure 2.2-14b Performance Comparison of 4-cell FETs with different processing output power and drain efficiency with 2.5W drive are shown.

(b) Wafer ML1-11E-9; Best overall devices without split-poly processing.



NOTES:

Bondwire support should be as close to the collector pad as possible

Figure 2.2-15 Assembly Diagram of 16W L-Band FET Showing Shunt-L Resonant Tuning on Both Input and Output. The Capacitors Shown are D.C. Blocking Elements in Series with the Tuning Inductors.

structure. Although all of these factors improved performance, efficiency improvements were less than we initially expected. As part of our effort to understand die performance, we used circuit models, including a non-linear SPICE model to simulate die performance.

Figure 2.2-16 shows a linear model based on measured DC and small signal parameters which were computer optimized to match measured S parameter data. This model was helpful in relating process changes to improvements in f_T and maximum available gain (MAG). These improvements did not always result in improved efficiency at rated power.

We used the MOSFET models available in our SPICE program, but could not obtain good agreement until we added a parasitic junction FET to the drain. The resulting structure is shown in Figure 2.2-17. The parasitic JFET is inherent in the DMOS design, and represents interference between two adjacent fingers within a cell. The proximity between the depletion regions of the adjacent fingers restricts the area of current flow in the drain, increasing resistive losses. Figure 2-2-18 shows measured and calculated drain characteristics using this model. The parasitic JFET reduces transconductance at large currents.

Figure 2.2-19 shows gain and efficiency calculated by the SPICE model. Saturated power and efficiency show good agreement with measured performance. Calculated gain is about 1 dB higher than measured gain. The improvements that would be expected if C_{RSS} and drain resistance could be

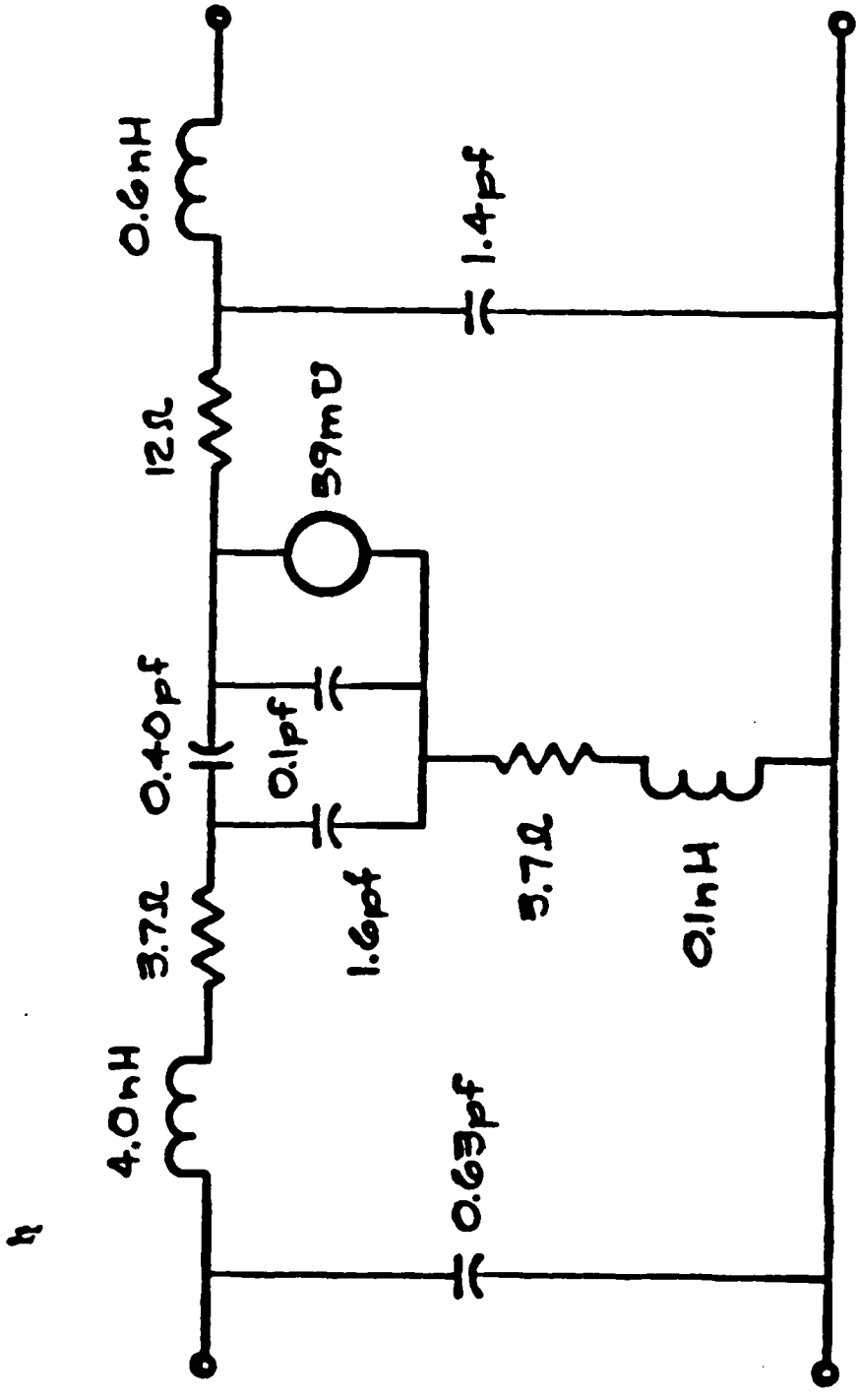


Figure 2.2-16 Small Signal Model of ML1 Cell.

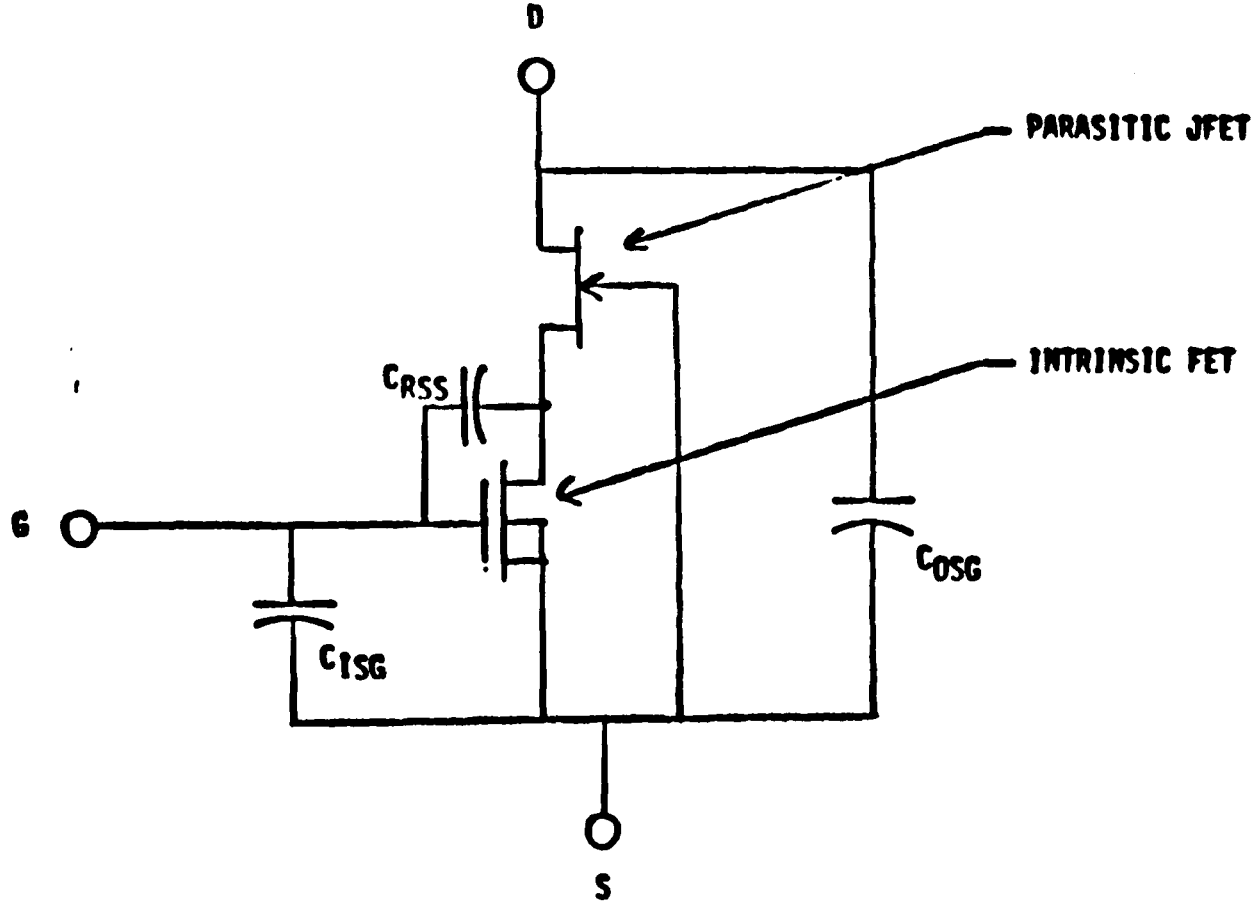


Figure 2.2-17 Spice Model of ML1. The parasitic JFET represents the current restriction in the drain due to adjacent fingers.

o Measured drain characteristics
——— Drain characteristics calculated from SPICE model
----- Load lines
(a) R_L = 16.5 ohms V_{DD} = 28V I_{DQ} = 0
(b) R_L = 36 ohms V_{DD} = 28V I_{DQ} = 200 ma

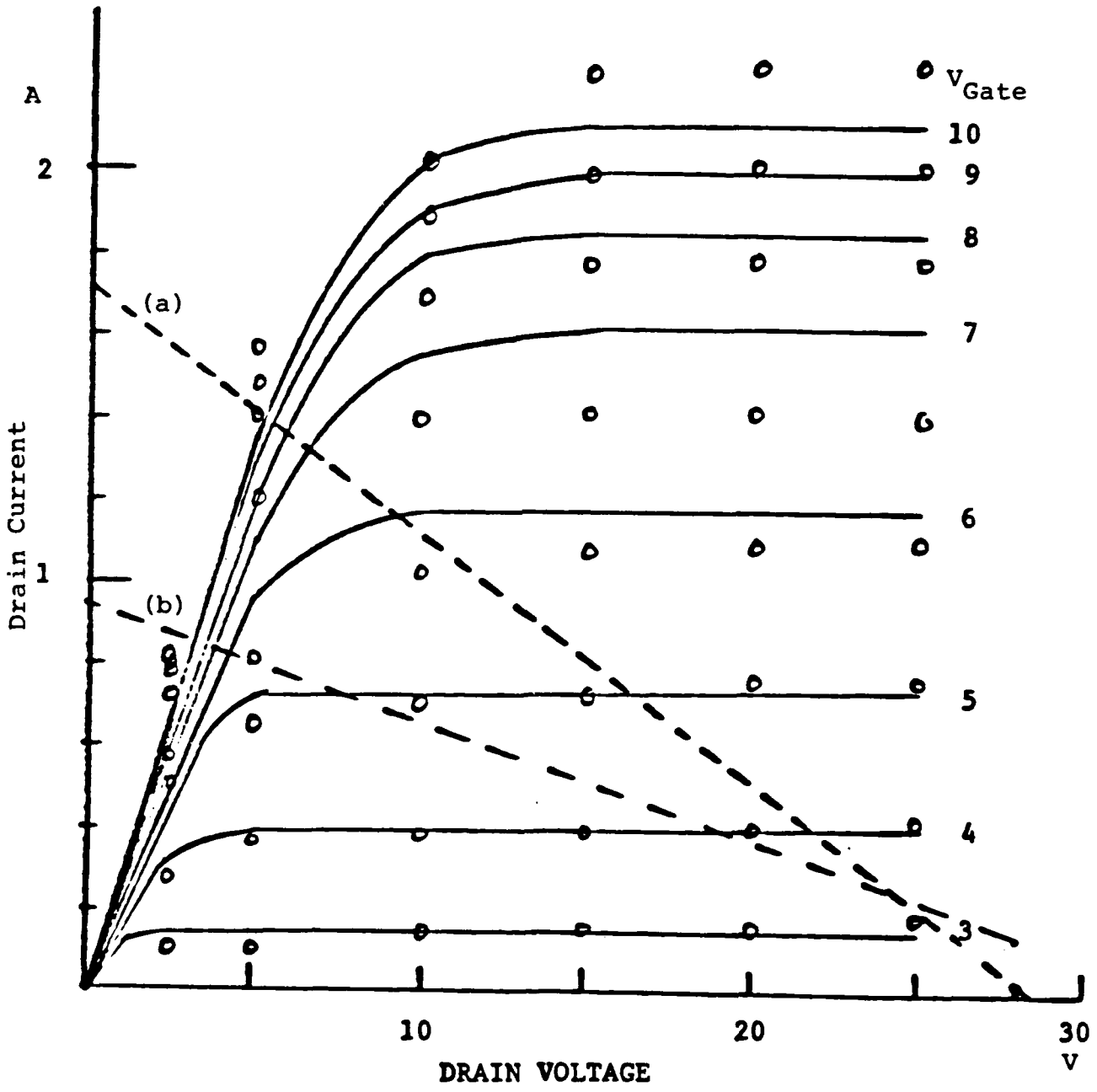


Figure 2.2-18 Measured Vs. Modelled DC Transfer Characteristics of 4-Cell ML1 MOSFET.

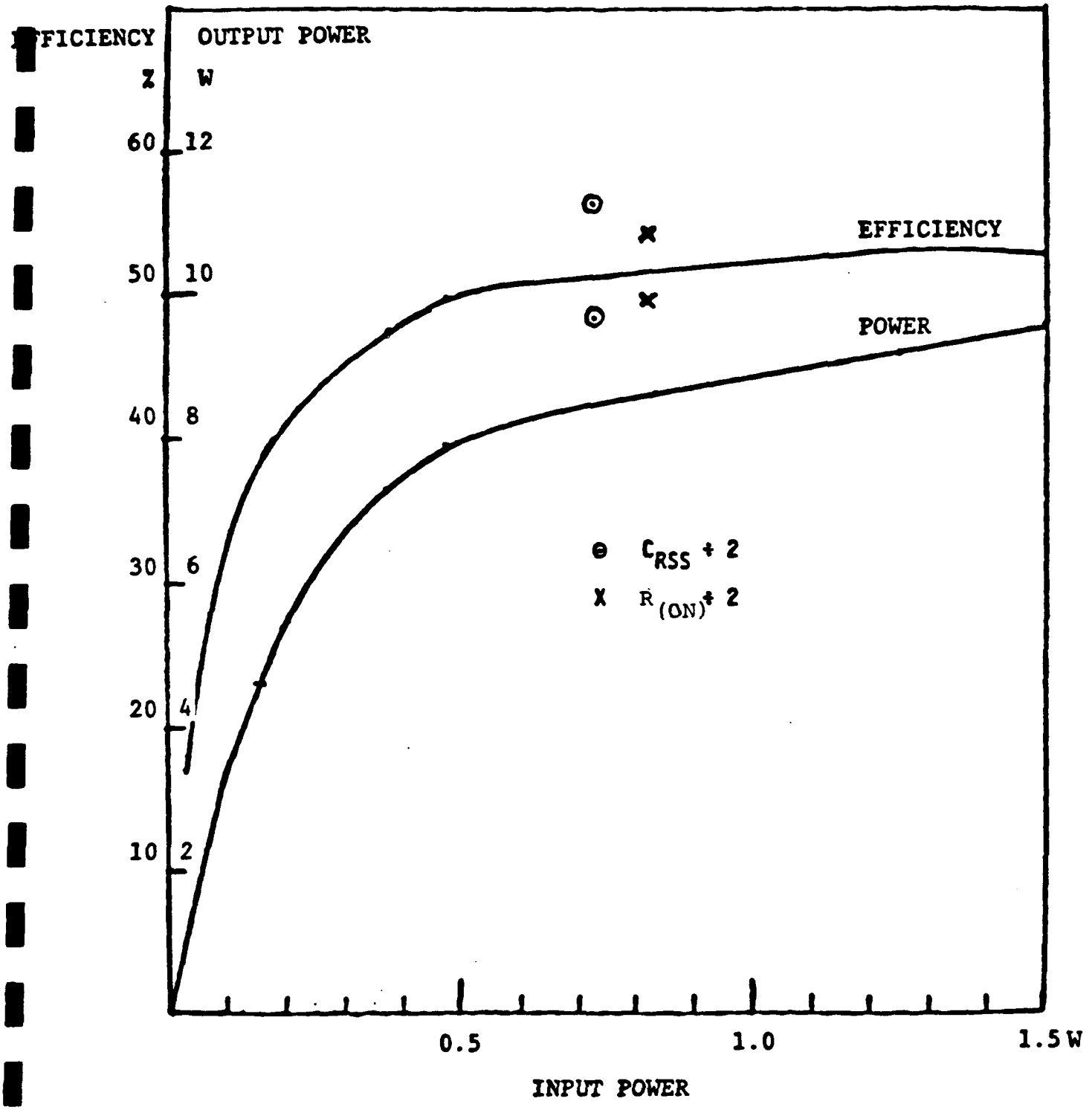


Figure 2.2-19 Calculated Power and Efficiency of 4-Cell ML1 Part. The SPICE calculations show good agreement with measured RF output power and efficiency and predict gains about 1 to 2 dB high. The calculated effects of reducing C_{RSS} or $R_{(ON)}$ are shown to illustrate the importance of these parameters.

further reduced is also shown.

We believe the ML1 DMOS device has been optimized to the point that little additional performance can be expected from the design, given current technology. One of the limiting factors was the parasitic JFET, and this appears to be the major factor controlling the maximum achievable efficiency.

Further increasing the gate width to source area ratio (analagous to the emitter periphery to base area of a bipolar transistor) to improve f_T and efficiency also has the effect of increasing the effect of the parasitic JFET. The final devices represent the optimum tradeoff between these effects.

2.2.5 Discussion of Delivered Devices

Within this contract there are three tasks. Ten devices were delivered representing the best result achieved in each task. In addition, alternate parts using some of the experimental processing developed during this contract, but not incorporated in the final devices, were included with the deliveries from Task II and III.

Figure 2.2-20 summarizes the deliveries.

2.2.5.1 Task I

The dice fabricated under Task I were 4 cell devices with no internal on-chip connections between cells, so that evaluation of individual cells was possible. Figure 2.2-21 shows DC and RF data of 14 devices, including the ten that were delivered. These are from wafer 2E-10, part of the

DELIVERABLE DEVICES

Task	Assembly Lot	Die Lot	Quantity	Fixture
I 1-2W cell	E5935	2E-10	10	862-441
II 1-2W optimized cell	E5962	11E-9 T5	10	862-441
	E5963	11E-20M	10*	862-441
III 10W L-Band FET	E5655 E5960	11E-9 T5) 11E-9 T5)	10	872-448
	E5964	19E-2 T5	5*	872-448

*Deliveries in addition to contract requirements.

FIGURE 2.2-20

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DATE: 12/19/86

D.C. TEST DATA

DIE TYPE ML1 ASSEMBLY LOT E5935

PACKAGE SS1 BONDING DIAGRAM Y-1208

WAFER NO. ML1-2E-10

SERIAL NUMBER	BVDSS 1mA (V)	I_{DSS} V_D=30	IGSS V_G=10 (uA)	GM V_D=10V I_D=100mA (mS)	$I_{D(ON)}$ V_G=10 V_D=2V (mA)	$V_{GS(th)}$ I_D=1mA (V)
1	75	25uA	< 1uA	80	220	2.3
2	75	< 1uA	< 1uA	90	225	2.5
3	76	< 1uA	< 1uA	78	215	2.2
4	76	< 1uA	< 1uA	85	220	2.3
5	76	< 1uA	< 1uA	85	220	2.5
6	76	< 1uA	< 1uA	85	220	2.6
7	76	< 1uA	< 1uA	80	220	2.4
8	76	< 1uA	< 1uA	85	225	2.5
10	76	< 1uA	< 1uA	85	225	2.4
11	76	< 1uA	< 1uA	84	220	2.5
12	76	< 1uA	< 1uA	82	220	2.4
13	77	< 1uA	< 1uA	86	225	2.3
14	75	< 1uA	< 1uA	88	225	2.6

FIGURE 2.2-21a. Task I FET Test Data, DC

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R.F. TEST DATA

PART NO. Y1208 CUST. _____ INITIAL: CCR

ASSEMBLY NO. E5935 TEST FIXTURE NO. 862-441 + Stubs

WAFER NO. MIL 2E-10 TEST CONDITIONS: 2mS 20% 28V

SERIAL NUMBER	FREQ. GHz	P_{IN} W	P_{OUT} W	GAIN dB	I_C A	η_D %	R_L dB	
1	1.4	.435	2.33	7.29	.191	43.6	11	
2	1.4	.435	2.5	7.60	.200	44.6	10	
3	1.4	.435	2.5	7.60	.199	44.9	10	
4	1.4	.435	2.33	7.29	.174	47.8	10	
5	1.4	.435	2.37	7.36	.173	48.9	9	
6	1.4	.435	2.37	7.36	.172	49.2	13	
7	1.4	.435	2.37	7.36	.173	48.9	12	
8	1.4	.435	2.45	7.51	.176	49.7	10	
9	1.4	.435	2.37	7.36	.190	44.6	12	
10	1.4	.435	2.45	7.51	.194	45.1	13	
11	1.4	.435	2.25	7.14	.185	43.4	9	
12	1.4	.435	2.37	7.36	.192	44.1	11	
13	1.4	.435	2.45	7.51	.195	44.9	11	
14	1.4	.435	2.5	7.60	.197	45.3	12	

FIGURE 2.2-21b. Task I FET Test Data, RF

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second lot processed. These parts used a 10 micron, 1 ohm centimeter epitaxial layer, as compared to the 14 micron, 1.2 ohm centimeter layer used in the devices from Lot 1. The cells produced about 2.3 W at 7.5 dB gain and 45 to 50% efficiency. Ruggedness was far more than necessary, indicating that there was much room for optimization by reducing the epitaxial resistivity and/or thickness. Decreasing the product of resistivity times epitaxial thickness $\rho.\ell$ improves gain, saturated power, and efficiently, but at the potential cost of loss of ruggedness and voltage handling capability.

2.2.5.2 Task II

Figure 2.2-22 shows DC and RF performance of devices developed under Task II. These devices are designated 11E-9, Type 5.

Wafer 11E-9 had the best RF power performance of all devices that could operate at 28V without ruggedness problems. These devices used a double-epitaxial structure consisting of 6 microns of 1 ohm - cm material over a graded buffer layer. This provided dramatically improved RF performance, still with excellent ruggedness and 28V operation capability. Typical performance was 8 dB gain at 4W output and over 60% efficiency. The "Type 5" cell was the best of the 4 cell variations evaluated. It used the medium value of polysilicon width, which provided the best compromise between minimizing capacitance, and minimizing the parasitic JFET in the drain. Type 5 also included a 40%

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D.C. TEST DATA

DIE TYPE ML1 TYPE 5 ASSEMBLY LOT E-5962

PACKAGE SS1 BONDING DIAGRAM Y-1208

WAFER NO. ML1-11E-9 TYPE 5

SERIAL NUMBER	BV_{DSS} 1mA (V)	I_{DSS} V_D=30	I_{GSS} V_G=10 (uA)	GM V_D=10V I_D=100mA (mS)	$I_{D(ON)}$ V_G=10 V_D=2V (mA)	$V_{GS(th)}$ I_D=1mA (V)
1	70	< 1uA	< 1	88	275	2.8
2	40s	.8mA	< 1	76	275	1.2
3	70	< 1uA	< 1	85	275	2.7
4	71	< 1uA	< 1	82	260	2.3
6	69	< 1uA	< 1	82	255	2.1
8	69	< 1uA	< 1	88	275	2.8
9	73	3uA	< 1	84	265	2.7
10	71	5uA	< 1	88	275	2.1
11	50s	70uA	< 1	80	265	1.6
15	18	< 1uS	< 1	86	265	2.7
16	74	4uA	< 1	90	275	2.8
19	72	< 1uA	< 1	88	260	2.7
20	65s	< 1uA	< 1	86	255	2.8

FIGURE 2.2-22a. Task II FET Test Data, DC

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R.F. TEST DATA

DATE: 12-19-86

PART NO. Y1208 CUST. N.R.L. INITIAL: CCR

ASSEMBLY NO. E5962 TEST FIXTURE NO. 862-441

WAFER NO. MIL 11E-9 Type 5 TEST CONDITIONS: 2mS 20% 28V I_Q = 5ma

SERIAL NUMBER	FREQ. GHz	P_{IN} W	P_{OUT} W	GAIN dB	I_C A	η_D %	R_L dB	
1	1.4	.588	4.0	8.3	.231	61.8	14	
2	1.4	.636	4.0	8.0	.223	64.1	20	
3	1.4	.588	3.66	7.9	.232	56.3	5	
4	1.4	.610	4.0	8.2	.238	60.0	12	
6	1.4	.592	4.0	8.3	.233	61.3	15	
8	1.4	.614	4.0	8.1	.232	61.6	15	
9	1.4	.584	4.0	8.4	.239	59.8	14	
10	1.4	.586	4.0	8.3	.238	60.1	11	
11	1.4	.600	4.0	8.2	.234	61.1	15	
15	1.4	.586	4.0	8.3	.230	62.1	11	
16	1.4	.622	4.0	8.1	.229	62.4	15	
18	1.4	.590	4.0	8.3	.245	58.3	11	
19	1.4	.586	4.0	8.3	.238	60.0	11	
20	1.4	.610	4.0	8.2	.230	62.1	15	

FIGURE 2.2-22b. Task II FET Test Data, RF

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larger cell size than the other types. The larger cell had less thermal capability per unit area than the other types. However, its excellent performance showed that the benefits of the increased size and the consequent reduction in MOS bond pad capacitance per unit cell area outweighed any thermal penalty. The 11E-9, Type 5 parts were also used in the Task III cell combining effort.

During Task II, a large number of processing variations were implemented and evaluated in addition to those used in wafer 11E-9. These were described earlier in this report. Ten devices from wafer 17E-20 were delivered in addition to the Task II contract requirement. Figure 2.2-23 shows results achieved from these devices. Gain shown is 8 dB at 62 to 65% efficiency. The parts could also be tuned for over 10 dB gain at 53% efficiency. These measurements are at 20 volts DC. Even higher gains were measured at 24 volts, but the parts could not pass a 3:1 VSWR test, a minimum ruggedness requirement for cells to be power-combined. As a result, 20V operation of these parts is required, and output power is reduced to 2.7-2.8W. Although this meets the 1-2W per cell goal of the contract, the wafer 11E-9 parts with 4W at 28V were considered our primary result from Task II.

The 17E -20M parts used split-poly processing, as described earlier, to reduce parasitics, and a 0.8 ohm-cm epitaxial layer to reduce the $\rho.\ell$ product. The "M" designation indicates that the polysilicon gate fingers are

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D.C. TEST DATA

DIE TYPE ML1 ASSEMBLY LOT E-5963

PACKAGE SS1 BONDING DIAGRAM Y-1208

WAFER NO. ML1-17E-20M

SERIAL NUMBER	BVDSS 1mA (V)	I_{DSS} V_D=30	I_{GSS} V_G=10 (uA)	GM V_D=10V I_D=100mA (mS)	$I_{D(ON)}$ V_G=10 V_D=2V (mA)	$V_{GS(th)}$ I_D=1mA (V)
4	55s	2uA	< 1	96	350	2.3
5	55s	< 1uA	< 1	98	375	2.0
6	53s	< 1uA	< 1	96	350	2.3
7	57s	< 1uA	< 1	96	350	2.3
8	57s	30uA	< 1	98	350	2.4
9	52s	2uA	< 1	98	365	2.1
10	52	< 1uA	< 1	98	350	2.1
11	53s	< 1uA	< 1	98	350	2.1
12	5		< 1			Failure
13	47	50uA	< 1	98	350	2.0
14	52s	< 1uA	< 1	100	360	2.1
15	52s	< 1uA	< 1	100	360	2.2
16	60s	< 1uA	< 1	98	350	2.4

NOTE: s = soft breakdown

FIGURE 2.2-23a. D.C. Test data of Additional Task II FETs.

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2	1.4	.435	2.83	8.13	.218	64.9	13
4	1.4	.435	2.83	8.13	.223	63.9	9
5	1.4	.435	2.57	7.71	.210	61.2	18
6	1.4	.435	2.70	7.93	.216	62.5	8
7	1.4	.435	2.74	7.99	.222	62.3	10
8	1.4	.435	2.74	7.99	.219	62.7	10
10	1.4	.435	2.66	7.86	.214	62.3	8
11	1.4	.435	2.83	8.13	.220	64.3	10
13	1.4	.435	2.53	7.65	.206	61.4	9
14	1.4	.435	2.86	8.17	.225	63.6	10
15	1.4	.435	2.79	8.07	.215	64.9	9
16	1.4	.435	2.83	8.13	.225	62.9	10

metallized. While this step is standard for the non-split-poly parts such as 11E-9, we attempted to eliminate it in split-poly parts because of its increased difficulty. However, this incurred a substantial gain and power penalty.

2.2.5.3 Task III

Task III was the development of a 10W-FET covering the 1.215-1.4 GHz band. Figure 2.2-24 shows DC and RF performance of the wafer 11E-9 parts which are the primary product of this effort. Typical performance is greater than 13W output at 7.2 to 7.7 dB gain and 53% to 57% efficiency across the band. Some parts exceed 55% efficiency at all frequencies. The design of the part was described earlier in the report. The parts use internal input and output matching to achieve the results described. The output match is a conventional shunt-L type, common on bipolar transistors. The input match is also a shunt-L type, unique to this FET. Unlike a bipolar die, this FET has a capacitive input impedance. A shunt-L input match therefore does a better job of raising the real part of the die impedance to a practical value than does the low-pass structure normally used with bipolar devices.

Figure 2.2-25 shows DC and RF performance of additional devices delivered. These devices are slightly lower in gain, with comparable power and efficiency to the primary devices. They have been delivered to demonstrate the capability of dice with split-poly processing. These dice are similar to the 27E-20 dice described earlier, but have

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R.F. TEST DATA

PART NO. Y1337 CUST. N.R.L. INITIAL: WL

ASSEMBLY NO. E5655 TEST FIXTURE NO. 872-448

WAFER NO. ML1-11E-9 TEST CONDITIONS: 2mS, 20%, 28V IQ=5mA

SERIAL NUMBER	FREQ. MHz	P_{IN} W	P_{OUT} W	GAIN dB	I_C A	Drain Eff. %	R_L dB	
3	1400	2.5	14.35	7.6	.939	54.6	18	
	1300		16.0	8.1	1.00	57.0	12	
	1215		14.0	7.5	.952	52.5	12	
4	1400		14.05	7.5	.935	53.7	18+	
	1300		15.75	8.0	.994	56.6	15	
	1215		13.55	7.3	.923	52.4	11	
5	1400		13.84	7.4	.902	54.6	16	
	1300		15.2	7.8	.944	57.7	10	
	1215		13.1	7.2	.904	51.7	11	
6	1400		13.6	7.4	.916	53.0	18+	
	1300		15.4	7.9	.992	55.4	18+	
	1215		13.2	7.2	.922	51.1	10	
9	1400		14.2	7.5	.922	55.0	18+	
	1300		16.0	8.1	1.00	57.0	13	
	1215		14.0	7.5	.956	52.3	12	
10	1400		12.8	7.1	.811	56.3	16	
	1300		15.0	7.8	.968	55.3	15	
	1215		12.8	7.1	.951	48.0	10	
11	1400		14.1	7.5	.915	55.0	18+	
	1300		15.7	8.0	.974	57.6	13	
	1215		14.05	7.5	.924	54.3	16	

FIGURE 2.2-24a . RF TEST DATA of Task III FETs

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R.F. TEST DATA

DATE: 6-10-87

PART NO. Y1337 CUST. N.R.L. INITIAL: WL

ASSEMBLY NO. E5960 TEST FIXTURE NO. 872-448

WAFER NO. ML1-11E-9 TEST CONDITIONS: 2mS, 20%, 28V, IQ=5mA

SERIAL NUMBER	FREQ. MHz	P_{IN} W	P_{OUT} W	GAIN dB	I_C A	η_D %	R_L dB	
1	1400	2.5	13.5	7.3	.832	57.9	10	
	1300	2.5	15.0	7.8	.904	59.3	8	
	1215	2.5	13.15	7.2	.876	53.6	7	
2	1400	2.5	13	7.2	.834	55.7	18	
	1300	2.5	13.65	7.4	.860	56.7	8	
	1215	2.5	13.15	7.2	.872	53.8	9	
7	1400	2.5	13.85	7.4	.874	56.6	8	
	1300	2.5	14.9	7.8	.925	57.5	10	
	1215	2.5	12.5	7.0	.852	52.4	6	
8	1400	2.5	13.15	7.2	.825	56.9	8	
	1300	2.5	14.4	7.6	.877	58.6	8	
	1215	2.5	13	7.2	.840	55.3	7	
9	1400	2.5	14.6	7.7	.943	55.3	12	
	1300	2.5	15.95	8.0	.980	58.1	7	
	1215	2.5	14.25	7.6	.946	53.8	10	
10	1400	2.5	14	7.5	.917	54.5	14	
	1300	2.5	15.5	7.9	.962	57.5	11	
	1215	2.5	13.45	7.3	.912	52.7	9	

FIGURE 2.2-24a (Continued) RF TEST DATA of Task III FETs

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D.C. TEST DATA

DIE TYPE ML1 ASSEMBLY LOT E5655

PACKAGE P31B BONDING DIAGRAM Y1337

WAFER NO. 11E-9

SERIAL NUMBER	BVDSS 1mA (V)	I_{DSS} V_D=30	I_{GSS} V_G=10 (uA)	GM V_D=10V (mS)	$I_{D(ON)}$ V_G=10 V_D=2V (mA)	
3	72	0	0	400	.90	
4	72	0	0	380	.80	
5	69	0	0	360	.86	
6	71	0	0	360	.80	
7	70	0	0	360	.90	
9	72	0	0	360	.92	
10	72-10mA	2.5	0	380	.80	
11	70	0	0	380	.95	

FIGURE 2.2-24b. DC TEST DATA of Task III FETs

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D.C. TEST DATA

DIE TYPE ML1 ASSEMBLY LOT E5960

PACKAGE P31B BONDING DIAGRAM Y1337

WAFER NO. ML1-11E-9

SERIAL NUMBER	BVDSS 1mA (V)	IDSS VD=30	IGSS VG=10 (uA)	GM VD=10V ID=1A (mS)	ID(ON) VG=10 VD=2V (mA)	VGS(th) VG=VD ID=1mA (V)
1	71	0	0	350	0.7	2.5
2	61	.1	0	300	0.75	2.4
7	72	0	0	400	0.8	2.6
8	56	0	0	350	0.7	2.2
9	71	0	0	350	0.7	3.2
10	71	0	0	400	0.7	3.3

FIGURE 2.2-24b. DC TEST DATA of Task III FETs (Continued)

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M/A-COM PHI, INC.

DATE: 6-10-87

R.F. TEST DATA

PART NO. YI337 CUST. N.R.L. INITIAL: WL

ASSEMBLY NO. E5964 TEST FIXTURE NO. 872-448

WAFER NO. ML1-19E-2T5 TEST CONDITIONS: 2mS, 20%, 28V, IQ=5mA

SERIAL NUMBER	FREQ. MHz	P_{IN} W	P_{OUT} W	GAIN dB	I_C A	Drain Eff. %	R_L dB	
1	1400	2.5	10.8	6.0	.748	51.6	18	
	1300		12.25	6.9	.817	53.6	18	
	1215		12.05	6.8	.822	52.4	16+	
2	1400		13.5	7.3	.856	56.3	18	
	1300		14.5	7.6	.926	56.0	10	
	1215		13.5	7.3	.914	52.8	14	
3	1400		10.7	6.3	.722	52.7	13	
	1300		12.1	6.8	.809	53.6	18+	
	1215		12.0	6.8	.804	53.3	16	
4	1400		12.7	7.0	.835	54.3	17	
	1300		14.6	7.7	.927	56.0	18+	
	1215		13.0	7.2	.892	52.2	16+	
5	1400		13.0	7.2	.859	54.0	18	
	1300		14.8	7.7		55.7	18+	
	1215		13.0	7.2	.930	49.9	16+	
6	1400		12.0	6.8	.971	43.9	14	
	1300		13.7	7.4	1.059	46.4	18	
	1215		13.3	7.3	1.048	45.1	16+	
7	1400		12.74	7.1	.833	54.7	17	
	1300		14.5	7.6	.917	56.4	17	
	1215	↓	12.8	7.1	.915	50.0	16+	

FIGURE 2.2-25a. RF TEST DATA OF ADDITIONAL PARTS AS DESCRIBED IN THF TEXT

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R.F. TEST DATA

DATE: 6-10-87

PART NO. Y1337 CUST. N.R.L. INITIAL: WL

ASSEMBLY NO. E5964 TEST FIXTURE NO. 872-448

WAFER NO. ML1-19E-2 TEST CONDITIONS: 2mS, 20%, 28V IQ=5mA

SERIAL NUMBER	FREQ. MHz	P_{IN} W	P_{OUT} W	GAIN dB	I_C A	Drain Eff. %	R_L dB	
9	1400	2.5	12.5	7.0	.849	52.6	11	
"	1300		14.2	7.5	.937	54.3	18+	
	1215		12.5	7.0	.877	50.9	16	
10	1400		13.0	7.2	.848	54.7	18+	
	1300		14.4	7.6	.940	54.5	14	
	1215	↓	13.0	7.2	.936	49.6	16+	

FIGURE 2.2-25a. RF TEST DATA OF ADDITIONAL PARTS AS DESCRIBED IN THE TEXT (continuation)

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M/A-COM PHI, INC.

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D.C. TEST DATA

DIE TYPE ML1 ASSEMBLY LOT E5964

PACKAGE P31B BONDING DIAGRAM Y1337

WAFER NO. ML1-19E-2

SERIAL NUMBER	BV_{DSS} 1mA (V)	I_{DSS} V_D=30	I_{GSS} V_G=10 (uA)	GM V_D=10V ID=1A (mS)	$I_{D(ON)}$ V_G=10 V_D=2V (mA)	$V_{GS(th)}$ VG=VD I_D=1mA (V)
1	69	0	0	250	0.7	3.1
2	67	0	0	400	0.8	3.1
3	67	0	0	300	0.8	3.1
4	66	0	0	400	0.85	3.3
5	67	0	0	400	0.8	3.2
6	67	0	0	400	0.85	3.1
7	68	0	0	400	0.85	3.3
9	66	0	0	350	0.85	3.2
10	69	0	0	400	0.85	3.3

FIGURE 2.2-25b. DC TEST DATA OF ADDITIONAL PARTS AS DESCRIBED IN THE TEST

FORMERLY POWER HYBRIDS, INC.

slightly less gain, but improved ruggedness and voltage capability. In addition, these parts are gold metallized.

2.2.5.4 Delivery Summary

The 10W L-band FETs in Figure 2.2-24 exceed the power and gain goals for this program. Some of the parts fall below the 55% efficiency goal over part of the band. These parts are internally matched devices from wafer 11E-9, type 5, judged the best overall dice fabricated during this effort. Additional parts were shipped to demonstrate parts using processes developed, but not incorporated into these devices, including split-poly processing and gold metallization.

3.0 RECOMMENDATIONS

The primary goals of this contract were twofold. Tasks I and II required developing a new 1 to 2 Watt silicon MOSFET die and optimizing it with respect to epitaxial, metallization and passivation parameters. Of particular concern was the development of a gold metallized FET because of its reliability advantages. Task III required development of a 10W L-Band MOSFET based on the results of Tasks I and II and demonstrating performance comparable to that of TPS-59 devices.

These goals have been met. A MOSFET has been developed that initially showed 1-2 Watts at L-Band frequencies, and after optimization it produced 3-5 Watts. Gold metallized FETs were developed and delivered.

A 10 watt L-Band MOSFET was developed which had performance at the 10-15 Watt output level comparable to that of bipolar transistors used in the TPS-59 power amplifier.

Extensive optimization of epitaxial structure, channel length, and cell layout resulted in devices which we believe approach the limits of performance achievable with this technology. In particular, further increases in gain, bandwidth, and efficiency will depend upon increases in channel mobility, decrease in channel length, or elimination of the parasitic JFET in the MOSFET drain.

Since the completion of the work described in this report, M/A-COM PHI has addressed these issues with a new geometry, the Rectangular Etched Silicon Field Effect

transistor (RESFET) which represents an extension of the DMOS technology, and an assault on the performance limits encountered during this contract. The key features of the RESFET are:

- Channel conduction in the 100 crystalline direction. This is the direction having the highest mobility.
- Diffusion-depth defined channel length. The channel is defined by diffusion into the bulk silicon rather than an edge defined by photolithography. It is therefore not limited by mask defects.
- No parasitic JFET. Because channels are perpendicular to the silicon surface there is no interactions between adjacent fingers which leads to "pinch off" in the drain on DMOS structures.

Use of the RESFET structure has resulted in improvements beyond that reported here. However, these structures have not been optimized with respect to epitaxial layer structure or diffusion profile.

The channel doping profile should be optimized to provide maximum voltage capability with minimum length, not subject to restriction due to mask edge defects. The RESFET structure provides for a higher gate width to source area ratio, which increases the power density in the chip. For a given duty cycle, heat removal becomes more important, and this affects the optimum cell layout.

We believe a careful optimization study of the RESFET design, similar to the optimization work applied in this contract to the ML1 would be valuable. Continued work should be targeted toward well defined applications. The results of such an effort would depend upon such factors as bandwidth, duty cycle, voltage and required linearity in the intended application. While the knowledge of various tradeoffs obtained during the effort would be valuable in future developments, the actual device might be of limited use unless the optimization effort is targeted for a specific application/system.

APPENDIX A

STATEMENT OF WORK
FOR
L-BAND POWER MOSFET

1.0 INTRODUCTION

1.1 General Statement

a) Work shall consist of developing an L-band MOSFET for TPS-59 phased array radar applications. Power MOSFETs offer the possibility of higher frequency, easier power combining and greater gain at L-band over bipolar technologies.

b) Work shall be completed over an eighteen month time frame.

1.2 Background

a) UHF power MOSFET's have only recently become available for high frequency applications.

b) L-band power MOSFET's are still in development and are not readily available to the industry. However, it has been shown that greater gain can be achieved in addition to eliminating complex circuit designs.

c) If the advantages of the power MOSFET at VHF and UHF frequencies with respect to performance and ease of circuit design can be projected to L-band, then there will be a significant positive impact for the future of L-band phased array radars, considering performance and cost.

d) Available microwave power MOSFET's are constructed employing aluminum metalization. Since gold has been a standard in the microwave industry because of enhanced reliability, there exists a need for gold metalized microwave power MOSFET's.

1.3 Purpose

a) To develop a medium power L-band MOSFET whose building block die can produce a device similar in performance to the TPS-59 bipolar transistor, typically a 3:1 VSWR variation across the band and 55-60% efficiency.

b) To employ refractory gold die metalization, and to assess device reliability.

1.4 Objectives

a) This eighteen month program has the following objectives:

1) Develop a low power L-band MOSFET to demonstrate capability. Evaluate gold metalization at this stage.

2) Optimize the low power L-band MOSFET in order to meet P_{SAT} requirements at a VSWR of 3:1.

3) Develop a medium power MOSFET based on the above optimization and power combining techniques in order to attain power output of 10 watts.

2.0 TECHNICAL REQUIREMENT

2.1 General

2.1.1 Tasks considered for this program could be considered high risk and developmental.

2.1.2 Previously developd proprietary technologies shall be identified prior to the start of this program.

2.1.3 A polysilicon gate lateral CMOS structure shall be employed in an interdigitated layout as a starting point for the power MOSFET development. The die will be constructed employing self aligning techniques to define the gate polysilicon, source contact and diffusions. Both dry etch and etchback techniques will be incorporated. The polysilicon gate will allow gold metalization which will be defined with ion milling techniques.

2.2 Tasks

2.2.1 Task I - Develop a 1-2 watt L-band MOSFET cell. This device will illustrate the capablity of the design and will not necessarily be optimized for performance. The device should be targeted for a minimum of 10 db gain in the TPS-59 frequency band at a VSWR of 3:1.

2.2.2 Task II - Develop a 1-2 watt L-band MOSFET that has been optimized with respect to epitaxial, metallization and passivation considerations.

2.2.3 Task III - Develop a 10 watt L-band MOSFET based on the results of task 2.2.2 with a minimum of 0.5 db combining losses, and efficiency of 55-60%.

3.0 DELIVERABLES

3.1 The contractor shall provide 10 L-band devices at the conclusion of each task. Appropriate test fixtures are to be included so that total device characteristcs may be carried out at NRL.

3.2 The contractor shall deliver all process instructions and drawings developed under this program.

3.3 The contractor shall deliver monthly letter type progress reports.

3.4 The contractor shall prepare a final report documenting all aspects of the program.

4.0 MEETINGS

4.1 The contractor shall conduct three on-site status reviews.

4.2 The contractor shall conduct two interim debriefings to be held at the Naval Research Laboratory.

4.3 The contractor shall conduct an end-of-contract briefing.